TITLE

PROCESS FOR PRODUCTION OF SEMICONDUCTOR SUBSTRATE

BACKGROUND OF THE INVENTION

[0001] This application is a continuation-in-part of application number 09/161,775 filed September 29, 1998, pending, which was a division of application 08/863,717 filed May 27, 1997, now U.S. Patent 5,856,229, which was a continuation of application number 08/401,237 filed March 9, 1995, abandoned. These applications also claim priority to Japanese patent applications 39389/94 and 45441/95 filed March 10, 1994 and March 6, 1995, respectively. This application is also a continuation-in-part of pending application number 09/734,667 filed December 13, 2000 which was a division of application number 09/212,432, filed December 16, 1998, now issued as U.S. Patent 6,246,068, which was a division of application number 08/729,722 filed October 7, 1996, now U.S. Patent 5,854,123. These applications claim priority to Japanese patent application 260100/95 filed October 6, 1995.

[0002] This application is also a continuation-in-part of pending application number 09/933,711, filed August 22, 2001, which was a division of application 09/840,895 filed April 25, 2001,now allowed, which was a division of application number 08/807,604 filed February 27, 1997, now issued as U.S. Patent 6,294,478.

These applications claim priority to Japanese application 41709/96 filed February 28, 1996.

[0003] All the above applications and their disclosures are incorporated herein by reference.

Field of the Invention

[0004] The present invention relates to a process for producing a semiconductor substrate. More specifically, the present invention relates to a process for producing a monocrystalline semiconductor on a dielectric-isolated or insulative material, or a monocrystalline compound semiconductor on a semiconductor substrate. Further the present invention relates to a process for producing an electronic device or an integrated circuit formed on a single crystalline semiconductor layer.

[0005] The present invention relates to a semiconductor substrate and a producing method thereof. More specifically, the present invention relates to dielectric isolation or .a producing method of a single-crystal semiconductor on an insulator and a single-crystal compound semiconductor on a Si substrate, and further relates to a method of producing a semiconductor substrate suitable for an electronic device or an integrated circuit formed at a single-crystal semiconductor layer.

[0006] The present invention relates to a fabrication process for a semiconductor substrate and, more particularly, to a process for fabricating a single-crystal semiconductor on a dielectric isolation or an insulator and a single-crystal compound semiconductor on a Si substrate and further to a process for fabricating a semiconductor substrate suitable for electronic devices and integrated circuits made in a single-crystal semiconductor layer.

Related Background Art

[0007] The technique of formation of monocrystalline Si (silicon) semiconductor on an insulative material is well known as silicon-on-insulator (SOI) technique. A device prepared by the SOI technique has various advantages which are not achievable by a bulk Si substrate in usual Si integrated circuits, as noted below:

1. Ease of dielectric isolation, and possibility of high degree of integration;

2. High resistance against radioactive ray;

3. Low floating capacity, and the possibility of high speed operation;

4. The welling process is unnecessary;

5. Preventability of latch-up; and

6. Possibility of producing a complete depletion type field-effect transistor to name a few.

[0008] The process of forming the SOI structure has been actively studied for several decades. The results of the studies are summarized, for example, in the paper: Special Issue; "Single-crystal silicon on non-single-crystal insulators"; edited by G.W. Cullen, Journal of Crystal Growth; Vol .63, No.3, pp.429-590 (1983).

[0009] SOS (silicon on sapphire) is known and is produced by heteroepitaxial growth of silicon on monocrystalline sapphire by CVD (chemical vapor deposition). The SOS technique, which is successful as one of SOI techniques, is limited in its application, because of many crystal defects caused by mismatch of

the lattice at the interface between the Si layer and the underlying sapphire, contamination of the Si layer with aluminum from the sapphire substrate, expense of the substrate, and the difficulty of large-area substrate formation.

[0010] Recently, studies are being made to produce the SOI structure without using a sapphire substrate. The studies are classified roughly into the two processes below:

1. A first process which includes surface oxidation of a monocrystalline Si substrate, local exposure of the Si substrate by opening a window, and epitaxial growth of Si laterally from the exposed portion as the seed to form an Si layer on SiO_2. (Si layer deposition on SiO_2.)

2. A second process including SiO_2 formation beneath a monocrystalline SiO_2 substrate, utilizing the SiO_2 substrate as the active layer. (No Si layer deposition.)

[0011] The device formed on a compound semiconductor exhibits performances, such as high speed, and luminescence, which are not achievable by Si. Such types of devices are formed by epitaxial growth on a compound semiconductor substrate such as GaAs. The compound semiconductor substrate, however, has disadvantages of high cost, low mechanical strength, and difficulty in the formation of a large-area wafer. Accordingly, heteroepitaxial growth of a compound semiconductor on an Si wafer is being studied to attain low cost, high mechanical strength, and ease of production of a large-area wafer.

[0012] The above-known process 1 (Si layer deposition on SiO_2) includes methods of direct lateral epitaxial growth of monocrystalline Si layer by CVD; deposition of amorphous Si and subsequent heat treatment to cause solid-phase lateral epitaxial growth; melting recrystallization to grow monocrystalline layer on an SiO_2 by irradiation of amorphous or polycrystalline Si layer with a focused energy beam

such as an electron beam and laser beam; and a zone melting recrystallization in which a bar-shaped heater is moved to scan with a belt-like melt zone. These methods respectively have advantages and disadvantages, involving problems in process controllability, productivity, product uniformity, and product quality, and are not industrialized yet. For example, the CVD method requires sacrificial oxidation, giving low crystallinity in the solid-phase growth. The beam annealing method involves problems in processing time of focused beam scanning and in controllability of beam superposition and focusing. of the above methods, the zone melting recrystallization is the most advanced method, and is employed in relatively large scale integrated circuits. This method, however, still causes crystal defects in subgrain boundaries, and is not successful in the production of a minority carrier device.

[0013] The above known process 2 in which the Si substrate is not utilized as the seed for epitaxial growth includes the four methods below:

1. An oxidation film is formed on a monocrystalline Si substrate which has V-shaped grooves on the surface formed by anisotropical etching; a polycrystalline Si layer is deposited in a thickness approximate to that of the Si substrate on the oxidation film; and the back face of the Si substrate is ground to form a monocrystalline Si region isolated dielectrically by surrounding with the V-shaped grooves. This method involves problems in controllability and productivity in deposition of polycrystalline Si in a thickness of as large as several hundred microns, and in removal of the monocrystalline Si substrate by grinding at the back face to leave an isolated active Si layer only.

2. An SiO_2 layer is formed by ion implantation into a monocrystalline Si substrate (SIMOX: Separation by ion implanted oxygen). This is the most highly advanced method in view of the matching with the Si process. This method, however, requires implantation of oxygen ions in an amount of as much as 10^{18}

ions/cm^2, which takes a long time, resulting in low productivity and high wafer cost. Further, the product has many remaining crystal defects; and does not have satisfactory properties for the industrial production of a minority carrier device.

3. An SOI structure is formed by oxidation of porous Si for dielectric isolation. In this method, an N-type Si layer is formed in an island-like pattern on a P-type monocrystalline Si substrate surface by proton ion implantation (Imai, et al.: J. Crystal Growth, Vol. 63, p. 547 (1983)) or by epitaxial growth and patterning, and subsequently only the P-type Si substrate is made porous by anodic oxidation in an HF solution to surround the island-patterned N-type Si, and the N-type Si island is dielectrically isolated by accelerated oxidation. In this method, the isolated Si regions are fixed prior to the device process, which may limit the freedom of device design disadvantageously.

4. Different from the above conventional SOI formation, a method has recently come to be noticed in which a monocrystalline Si substrate is bonded to another thermally oxidized monocrystalline Si substrate by heat treatment or use of an adhesive to form an SOI structure. This method requires uniform thinness of the active layer for the device: namely, formation of a film of a micron thick or thinner from a monocrystalline substrate of several hundred microns thick. This thin film may be formed by either of the two methods below.

1. Thin film formation by grinding; and

2. Thin film formation by selective etching.

[0014] The grinding method does not readily give a uniform thin film. In particular, formation of a film of submicron thickness results in thickness variation of tens of percent. This irregularity is a serious problem. With a larger diameter of the wafer, the uniformity of the thickness is much more difficult to attain.

[0015] The etching method is regarded to be effective for uniform thin film formation. This method, however, involves the problems of insufficient selectivity of about 10^2 at the highest, inferior surface properties after etching, and low crystallinity of the SOI layer because of the employed ion implantation, epitaxial or heteroepitaxial growth on a high-concentration B-doped Si layer. (C. Harendt, et al.: J. Elect. Mater., Vol. 20, p. 267 (1991); H. Baumgart, et al.: Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp. 733 (1991); and C.E. Hunt: Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp. 696(1991))

[0016] The semiconductor substrate which is prepared by lamination requires two wafers essentially, and a major part of one of the wafers is discarded by grinding or etching, thereby wasting the resource. Therefore, the SOI prepared by lamination involves many problems in controllability, uniformity, production cost, and so forth in conventional processes.

[0017] A thin Si layer deposited on a light-transmissive substrate typified by a glass plate becomes amorphous or polycrystalline owing to disorder of crystallinity of the substrate, not giving high performance of the device. Simple deposition of Si does not give desired quality of single crystal layer owing to the amorphous crystal structure of the substrate.

[0018] The light-transmissive substrate is essential for construction of a light-receiving element such as a contact sensor, and projection type of liquid crystal image-displaying apparatus. Additionally, a driving element of high performance is necessary for higher density, higher resolution, and higher precision of the sensor and of the image elements of the display. Consequently, the element provided on a light transmissive substrate is also required to have a monocrystalline layer of high crystallinity.

[0019] Amorphous Si or polycrystalline Si will not give a driving element having the required sufficient performance because of the many defects in the crystal structure.

[0020] As mentioned above, a compound semiconductor device requires essentially a compound semiconductor substrate. The compound semiconductor substrate, however, is expensive, and is not readily formed in a larger size.

[0021] Epitaxial growth of a compound semiconductor such as GaAs on an Si substrate gives a grown film of poor crystallinity owing to the difference in the lattice constants and the thermal expansion coefficients, thereby the resulting grown film being unsuitable for use for a device.

[0022] Epitaxial growth of a compound semiconductor on porous Si is intended for mitigation of mismatch of the lattices. However, the substrate does not have sufficient stability and reliability owing to the low thermal stability and long-term deterioration of the porous Si.

[0023] In view of the above-mentioned problems, Takao Yonehara, one of the inventors of the present invention, disclosed formerly a novel process for preparing a semiconductor member in European Patent Publication No. 0469630A2. This process comprises the steps of forming a member having a nonporous monocrystalline semiconductor region on a porous monocrystalline semiconductor region; bonding the surface of a member of which the surface is constituted of an insulating substance onto the surface of the nonporous monocrystalline semiconductor region; and then removing the porous monocrystalline semiconductor region by etching. This process is satisfactory for solving the above-mentioned problems. Further improvement of the disclosed process for

higher productivity and lower production cost will contribute greatly to the industries concerned.

[0024] Formation of a single-crystal Si semiconductor layer on an insulator is widely known as a silicon on insulator SOI. This technique has been extensively researched since a device utilizing the SOI technique has a number of advantages which cannot be achieved by a bulk Si substrate forming the normal Si integrated circuit. Specifically, for example, the following advantages can be achieved by employing the SOI technique:

1. Dielectric isolation is easy and high integration is possible;

2. Radiation resistance is excellent;

3. Floating capacitance is reduced and high speed is possible;

4. Well process can be prevented;

5. Latch-up can be prevented; and

6. Fully depleted (FD) field effect transistor is achieved through film thickness reduction.

[0025] These are described in detail, for example, in the literature of Special Issue: "Single-crystal silicon on non-single-crystal insulators"; edited by G.W. Cullen, Journal of Crystal Growth, volume 63, no. 3, pp. 429-590 (1983).

[0026] Further, over the past few years, the SOI has been largely reported as a substrate which realizes the acceleration of a MOSFET and low power consumption (IEEE SOI conference 1994). Since an element has an insulating

layer at its lower part when employing the SOI structure, an element separation process can be simplified as compared with forming an element on a bulk silicon wafer so that preparing a device can take less time. Specifically, in addition to achieving the higher performance, reduction of the wafer cost and the process cost is expected as compared with a MOSFET or IC on bulk silicon.

[0027] Particularly, the fully depleted (FD) MOSFET is expected to achieve higher speed and lower power consumption through improvement in driving force. In general, a threshold voltage (Vth) of a MOSFET is determined by the impurity concentration at a channel portion. On the other hand, in case of the FD MOSFET using the SOI, a depletion layer is also subjected to an influence of a film thickness of the SOI. Thus, for producing the large scale integrated circuits at high yield, uniformity of the SOI thicknesses has been strongly demanded.

[0028] On the other hand, a device on a compound semiconductor has high performance, such as high speed and luminescence, which cannot be achieved by Si. Presently, such a device is normally formed in an epitaxial layer grown on a compound semiconductor substrate, such as a GaAs substrate.

[0029] However, there is a problem that the compound semiconductor substrate is expensive while low in mechanical strength, so that a large area wafer is difficult to produce.

[0030] Under these circumstances, an attempt has been made to achieve the heteroepitaxial growth of a compound semiconductor on a Si wafer which is inexpensive and high in mechanical strength so that a large area wafer can be produced.

[0031] Referring back to the SOI, research on the formation of the SOI substrates has been active since the 1970s. In the beginning, the research was performed in

connection with the SOS (sapphire on silicon) method, which achieves the heteroepitaxial growth of single-crystal silicon on a sapphire substrate being an insulator, the FIPOS (fully isolated by porous oxidized silicon) method, which forms the SOI structure by dielectric isolation based on oxidation of porous Si, and the oxygen ion implantation method.

[0032] In the FIPOS method, an n-type Si layer is formed on a surface of a p-type Si single-crystal substrate in an island shape through the proton ion implantation (Imai and collaborator, J. Crystal Growth, vol. 63, 547 (1983)) or through the epitaxial growth and the patterning, then only the p-type Si substrate is rendered porous so as to surround the Si island from the surface by means of the anodizing method in a HF solution, and thereafter the n-type Si island is dielectric-isolated through accelerating oxidation. In this method, there is a problem that the isolated Si region is determined in advance of the prepared device so that the degree of freedom of device designing is limited.

[0033] The oxygen ion implantation method is a method called SIMOX first reported by K. Izumi. After implanting about 10^{17} to $10^{18}/cm^2$ of oxygen ions into a Si wafer, the ion-implanted Si wafer is annealed at the high temperature of about 1,320°C. in the atmosphere of argon/oxygen. As a result, oxygen ions implanted with respect to a depth corresponding to a projection range (Rp) of ion implantation are bonded with silicon so as to form a silicon oxide layer. On this occasion, a silicon layer which has been rendered amorphous at an upper portion of the silicon oxide layer due to the oxygen ion implantation is also recrystallized so as to be a single-crystal silicon layer. Conventionally, there have been a lot of defects included in the silicon layer on the surface, that is, about $10^5/cm^2$. On the other hand, by setting an implantation amount of oxygen to about $4x10^{17}/cm^2$, defects are successfully reduced to about $10^2/cm^2$. However, since the ranges of implantation energy and implantation amount for maintaining the quality of the silicon oxide layer, the crystalline property of the surface silicon layer and the like

are so narrow that thicknesses of the surface silicon layer and the buried silicon oxide (BOX: buried oxide) layer were limited to particular values. For achieving a desired thickness of the surface silicon layer, it was necessary to perform sacrificial oxidation and epitaxial growth. In this case, there is a problem that, since the degradation caused through these processes is superimposed on the distribution of thicknesses, the thickness uniformity deteriorates.

[0034] It has been reported that a formation failure region of silicon oxide called a pipe exists in the BOX layer. As one cause of this, the forcing matter upon implantation, such as dust, is considered. In the portion where the pipe exists, the deterioration of the device characteristic results from leaks between an active layer and a support substrate.

[0035] Further, since the amount of ion implantation in the SIMOX is large as compared with the ion implantation in the ordinary semiconductor process, implantation time is lengthy even after developing the apparatus to be used exclusively for that process. The ion implantation is performed by raster-scanning an ion beam of a given current amount or expanding the beam so that an increment of the implantation time is predicted following an increment in the area of the wafer. Further, in the high temperature heat treatment of the large-area wafer, it has been pointed out that a problem of occurrence of slip due to the temperature distribution in the wafer becomes more severe. In SIMOX, the heat treatment is essential at high temperature, that is, 1,320°C., which is not normally used in silicon semiconductor processes, so that there has been concern that this problem, including the development of the apparatus, becomes more significant.

[0036] On the other hand, apart from the foregoing conventional SOI forming method, attention has been recently given to the method which forms the SOI structure by sticking a Si single-crystal substrate to a thermal-oxidized Si single-crystal substrate through heat treatment or using adhesives. In this method,

it is necessary to form an active layer for the device into a uniform film. Specifically, it is necessary to form a Si single-crystal substrate of a thickness of as much as hundreds of microns into a film of several microns or less. There are three kinds of methods for thickness reduction as follows:

1. Thickness reduction through polishing;

2. Thickness reduction through local plasma etching;

3. Thickness reduction through selective etching.

[0037] In polishing, uniform thickness reduction is difficult. Particularly, in the case of thickness reduction to submicrons, the irregularity amounts to as much as tens of percents so that uniformity is a big problem. If the size of the wafer is further enlarged, the difficulty is increased correspondingly.

[0038] In the second method, after reducing the thickness to about 1 to $3\mu m$ through polishing, the thickness distribution is measured at many points. Thereafter, by scanning the plasma using the SF6 of a diameter of several millimeters based on the thickness distribution, etching is performed while correcting the thickness distribution, to reduce the thickness to a given value. In this method, it has been reported that the thickness distribution can be within the range of about ±10nm. However, if foreign matter (particles) exists on the substrate upon plasma etching, the foreign matter works as an etching mask so that projections are formed on the substrate.

[0039] Since the surface is rough immediately after the etching, touch polishing is necessary after completion of the plasma etching. The polishing amount is controlled based on time management, and hence, the control of final film thickness and the deterioration of film thickness distribution due to polishing have

been noted. Further, in polishing, abrasives such as colloidal silica directly rub the surface working as an active layer so that there has been concern about formation of a fracture layer due to polishing and introduction of processing distortion. Further, if the wafer is substantially increased in area, since the plasma etching time is increased in proportion to increment of the wafer area, there is concern about extreme reduction of the throughput.

[0040] In the third method, a film structure capable of selective etching is formed in advance in a substrate to be formed into a film. For example a p+-Si thin layer containing boron in the concentration no less than $10^{19}/cm^3$ and a p^-- Si thin layer are formed on a p^- substrate using the method of, for example, the epitaxial growth to form a first substrate. The first substrate is bonded with a second substrate via an insulating layer such as an oxide film, and then the underside of the first substrate is ground or polished in advance so as to reduce its thickness. Thereafter, the p^+ layer is exposed through the selective etching of the p^- layer and further the p^- layer is exposed through the selective etching of the p^+ layer, so as to achieve the SOI structure. This method is detailed in the report of Maszara.

[0041] Although the selective etching is said to be effective for uniform thickness reduction, it has the following problems:

[0042] The ratio of etching selectively is 10^2 at most, which is not sufficient.

[0043] Since surface property after etching is bad, touch polishing is required after etching. However, as a result, the film thickness is reduced and the thickness uniformity tends to deteriorate. Particularly, although the amount of polishing is managed based on time, since dispersion of the polish speed is large, the control of the amount of polishing is difficult. Thus, it becomes a problem particularly in forming an extremely thin SOI layer of, for example, 100nm.

[0044] The crystalline property is bad because of using the ion implantation, the epitaxial growth or the heteroepitaxial growth on the high-concentration B doped Si layer.

[0045] The surface property of a surface to be bonded which is inferior to the normal silicon wafer (C. Harendt, et al., J. Elect. Mater. Vol. 20, 267 (1991), H. Baumgart, et al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp. 733 (1991), C.E. Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp. 696 (1991)). Further, the selectivity of selective etching largely depends upon a difference in concentration of impurities such as boron and sharpness of the profile in the depth direction. Accordingly, if the high-temperature bonding annealing for increasing the bonding strength or the high temperature epitaxial growth for improving the crystalline property is performed, the depth direction distribution of the impurity concentration expands so that the selectivity of etching deteriorates. That is, it is difficult to improve both the ratio of etching selectively and the crystalline property or the bonding strength.

[0046] Recently, in view of the foregoing problems, Yonehara and collaborators have reported the bonded SOI which is excellent in thickness uniformity and crystalline property and capable of batch processing. Brief explanation about this will be given using Figs. 33A to 33E. In this method, a porous layer 162 formed on an Si substrate 161 is used as a material for selective etching (Fig. 33A). After epitaxially growing a nonporous single-crystal Si layer 163 on the porous layer 162 (Fig. 33B), the three-layer composite is bonded with a support substrate 164 via the oxidized Si layer 163 (Fig. 33C). The Si substrate 161 is reduced in thickness through grinding or the like from the underside so as to expose the porous Si 162 all over the substrate. (Fig. 33D). The exposed porous Si 162 is removed through etching using a selective etching liquid, such as KOH or $HF+H_2O_2$ (Fig. 33E). At this time, since the ratio of etching selectively porous Si relative to bulk Si (nonporous single-crystal silicon) can be set fully high, that is, 100,000 times, the

non-porous single-crystal silicon layer grown on the porous layer in advance can be left on the support substrate without being hardly reduced in thickness, so as to form the SOI substrate. Accordingly, the thickness uniformity of the SOI is substantially determined during the epitaxial growth. Since a CVD apparatus used in the normal semiconductor process can be used for the epitaxial growth, according to the report of Sato and collaborator, the thickness uniformity is realized, for example, within 100nm ± 2%. Further, the crystalline property of the epitaxial silicon layer is also excellent and has been reported to be $3.5x10^2/cm^2$.

[0047] In the conventional method, since the selectivity of etching depends on the difference in impurity concentration and the depth direction profile, the temperature of the heat treatment (bonding, epitaxial growth, oxidation or the like) which expands the concentration distribution is largely limited to approximately no higher than 800°C. On the other hand, in the etching of this method, since the difference in structure between porous and bulk determines the etching speed, the limitation of the heat treatment temperature is small. It has been reported that the heat treatment at about 1,180°C. is possible. For example, it is known that the heat treatment after bonding enhances the bonding strength between the wafers and reduces the number and size of voids generated at the bonded interface. Further, in the etching based on such a structural difference, the particles, even if adhered on porous silicon, do not affect the thickness uniformity.

[0048] On the other hand, in general, on a light transmittable substrate, typically glass, the deposited thin Si layer only becomes amorphous or polycrystalline at best, reflecting disorder in crystal structure of the substrate, so that the high-performance device cannot be produced. This is due to the crystal structure of the substrate being amorphous, and thus an excellent single-crystal layer cannot be achieved even by merely depositing the Si layer.

[0049] However, the semiconductor substrate obtained through bonding normally requires two wafers one of which is removed, wastefully for the most part, through polishing, etching or the like, so that the finite resources of the earth are wasted.

[0050] Accordingly, in the conventional method, the bonded SOI has various problems of controllability, uniformity and economics.

[0051] Formation of a single-crystal Si semiconductor layer on an insulator is widely known as Si On Insulator (SOI) technology and much research has been focused thereon, because devices obtained utilizing the SOI technology have many advantages that cannot be achieved by the normal bulk Si substrates for fabrication of Si integrated circuits. Namely, use of SOI technology can enjoy the following advantages, for example:

1. Dielectric isolation is easy and high integration is possible.

2. Radiation resistance is high.

3. Stray capacitance is reduced and the operation speed can be enhanced.

4. The well process can be omitted.

5. Latch-up can be prevented.

6. Fully depleted field effect transistors can be fabricated by thin-film structure.

[0052] These advantages are described in further detail, for example, in the reference [Special Issue: "Single-crystal silicon on non-single-crystal insulators";

edited by G. W. Cullen, Journal of Crystal Growth, volume 63, no 3, pp 429-590 (1983)].

[0053] In recent years, many reports have been presented on the SOI as a substrate focused on increase of speed and decrease of consumption power of MOSFET (IEEE SOI conference 1994). Since the SOI structure has an insulating layer below the device, use thereof can simplify the device isolation process as compared with cases for forming the devices on a bulk Si wafer, which results in shortening the device process steps. Namely, in addition to the increase in performance, the total costs including the wafer cost and the process cost are expected to be lower than those of MOSFETs and ICs on bulk Si.

[0054] Among others, the fully depleted MOSFETs are expected to increase the speed and decrease the consumption power due to an improvement in driving force. The threshold voltage (Vth) of MOSFET is determined in general by an impurity concentration of the channel portion, and, in the case of the fully depleted (FD) MOSFETs using the SOI, the thickness of a depletion layer is also influenced by the film thickness of the SOI. Accordingly, evenness of the film thickness of SOI is highly desirable for fabricating large-scale integrated circuits with good yields.

[0055] On the other hand, the devices on a compound semiconductor have high performance that cannot be attained by Si, for example, high-speed operation, radiation of light, and so on. Presently, most of these devices are fabricated in a layer epitaxially grown on a compound semiconductor substrate of GaAs or the like. The compound semiconductor substrates, however, have problems such as high expense, low mechanical strength, difficulty in fabrication of a large-area wafer, etc.

[0056] Because of these problems, attempts have been made to hetero-epitaxially grow a compound semiconductor on the Si wafer, which is cheap, has high mechanical strength, and permits fabrication of a large-area wafer.

[0057] Returning to the SOI structure, research on formation of SOI substrates has been active since the 1970s. In the early stage, much research was focused on a method for hetero-epitaxially growing single-crystal Si on a sapphire substrate as an insulator (SOS: Silicon on Sapphire), a method for forming the SOI structure by dielectric isolation based on oxidation of porous Si (FIPOS: Full Isolation by Porous Oxidized Silicon), and an oxygen ion implantation method.

[0058] The FIPOS method is a method for forming an n-type Si layer in an island pattern on a surface of a p-type Si single-crystal substrate by proton implantation (Imai et al., J. Crystal Growth, vol 63, 547 (1983)) or by epitaxial growth and patterning, making only the p-type Si substrate porous from the surface, so as to surround Si islands by anodization in HF solution, and then dielectric-isolating the n-type Si islands by enhanced oxidation. This method has a problem in that degrees of freedom on device designing are limited, because the Si regions isolated are determined prior to the device processes.

[0059] The oxygen ion implantation method is called SIMOX, which was first reported by K. Izumi. Oxygen ions are first implanted in about 10^{17} to $10^{18}/cm^2$ into a Si wafer, and thereafter the wafer is annealed at a high temperature of approximately 1320 °C in an argon-oxygen atmosphere. As a result, the oxygen ions implanted around the depth corresponding to the projected range (Rp) of ion implantation are bound with Si to form an oxidized Si layer. At that point, a Si layer, amorphized by the oxygen ion implantation above the oxidized Si layer, is also recrystallized to form a single-crystal Si layer. Crystalline defects in the surface Si layer were as many as $10^5/cm^2$ before, but they were successfully decreased to below $10^2/cm^2$ by adjusting the amount of implantation of oxygen to

approximately 4 x $10^{17}/cm^2$. However, the film thicknesses of the surface Si layer and the buried, oxidized Si layer (BOX; Buried Oxide) were limited to specific values due to narrow ranges of implantation energy and implantation dose capable of maintaining the film quality of the oxidized Si layer, crystallinity of the surface Si layer, and so on. Sacrificial oxidation or epitaxial growth was necessary for obtaining the surface Si layer in a desired film thickness. In that case, there is a problem that evenness of film thickness is degraded, because degradation due to these processes is added on the distribution of film thickness.

[0060] It is also reported that malformed regions of oxidized Si called pipes exist in the BOX. One of the causes thereof is conceivably contaminations such as dust upon implantation. In the portions including the pipes, degradation of device characteristics occurs due to leakage between the active layer and the support substrate.

[0061] Since the implantation dose in the ion implantation of SIMOX is larger than in the ion implantation used for the normal semiconductor processes as described previously, the implantation time is still long even after dedicated equipment has been developed. Since the ion implantation is carried out by raster scan of an ion beam of a predetermined electric current amount or by expanding the beam, an increase in the implantation time is anticipated with an increase in the area of wafer. In high-temperature annealing of a large-area wafer, it is pointed out that the problem of generation of slip or the like due to the temperature distribution within the wafer becomes more severe. Annealing at high temperatures, such as 1320°C, which are not used normally in the Si semiconductor processes, is indispensable for the SIMOX, and there is thus such a concern that the above problem becomes more significant, including development of equipment.

[0062] Aside from the conventional SOI forming methods described above, attention has recently focused on another method for bonding a Si single-crystal

substrate to another Si single-crystal substrate thermally oxidized, by annealing or with an adhesive, thereby forming the SOI structure. This method requires evenly thinning the active layer for the device. In other words, it is necessary to thin the Si single-crystal substrate even several hundred μm thick down to the order of μm or less. The following three types of methods are available for this thinning:

(1) thinning by polishing

(2) thinning by localized plasma etching

(3) thinning by selective etching.

[0063] It is difficult to achieve uniform thinning by the polishing method of (1). In particular, several ten % of dispersion appears in thinning on the sub-μm order, and evening of this dispersion is a big problem. The degree of difficulty increases with further increases in the diameter of a given wafer.

[0064] The above method of (2) is used to thin the layer roughly by the method of polishing of (1) to about 1 to 3 μm and to measure a distribution of film thicknesses at multiple points over the entire surface. After that, based on this distribution of film thicknesses, the layer is etched to correct the distribution of film thicknesses by scanning it with a plasma using SF_6 or the like in the diameter of several mm, whereby the layer is thinned down to a desired film thickness. It is reported that this method can achieve the film thickness distribution of about ±10 nm. However, if there are contaminants (particles) on the substrate upon plasma etching, the contaminants will serve as an etching mask, thereby forming projections on the substrate.

[0065] Since the surface is rough immediately after etching, touch polishing is necessary after completion of the plasma etching. Control of the amount of

polishing is carried out by time management, and thus control of degradation of the final film thickness and of the film thickness distribution by polishing is possible. Further, because in polishing, an abrasive such as colloidal silica directly rubs the surface to become the active layer, concerns exist about formation of a crush layer and introduction of work strain by polishing. As the wafers further increase in area, the time for plasma etching also increases proportionally, which also raises another concern about an extreme drop of throughput.

[0066] The above method of (3) is a method for preliminarily forming a selectively etchable film structure in a substrate to be thinned. For example, a thin layer of p^+-Si containing boron in a concentration of 10^{19} or more /cm^3 and a thin layer of p-type Si are stacked on a p-type substrate by the method of epitaxial growth or the like, thereby obtaining a first substrate. This is bonded to a second substrate through an insulating layer of oxide film or the like and thereafter the back face of the first substrate is preliminarily thinned by grinding and polishing. After that, the p^+-layer is exposed by selective etching of the p-type substrate and the p-type thin layer is exposed by selective etching of the p^+-layer, thus completing the SOI structure. This method is described in detail in the report of Maszara (J. Electrochem. Soc. 138, 341 (1991)).

[0067] Although the selective etching is said to be effective for uniform thinning, it has the following problems:

- The etch selectivity is not sufficient, at most 10^2.

- It requires touch polishing after etching, because the surface flatness after etching is poor. This, however, results in a decrease in the film thickness and a tendency to degrade the uniformity of film thickness. Polish amounts are managed by polishing time, but polishing rates vary greatly, which makes controlling the

amount of polish difficult. Accordingly, a problem arises particularly in forming a very thin SOI layer, for example, 100 nm thick.

• Crystallinity of the SOI layer is poor due to use of ion implantation and epitaxial growth or hetero-epitaxial growth on the high-concentration-B-doped Si layer. The surface flatness of the bonded surfaces are inferior to normal Si wafers.

[0068] Thus, the method of (3) has the above problems (C. Harendt, et al., J. Elect. Mater. Vol. 20, 267 (1991), H. Baumgart, et al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-733 (1991); C. E. Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991)). Also, the selectivity of selective etching is greatly dependent on concentration differences of impurities of boron or the like and steepness of its depthwise profile. Therefore, if high-temperature bonding annealing is conducted in order to enhance the bonding strength or if high-temperature epitaxial growth is conducted in order to improve crystallinity, the depthwise distribution of impurity concentration will expand to degrade the etch selectivity. This illustrates the difficulty realizing both an improvement in etch selectivity and an improvement in bonding strength.

[0069] Recently, Yonehara et al., solving such problems, reported the bonding of SOI excellent in uniformity of film thickness and in crystallinity and capable of being batch-processed (T. Yonehara, K. Sakaguchi and N. Sato, Appl. Phys. Lett. 64, 2108 (1994)). This method uses a porous layer 242 on an Si substrate 241, as a material of selective etching. A non-porous single-crystal Si layer 243 is epitaxially grown on the porous layer and thereafter it is bonded to a second substrate 244 through an oxidized Si layer 245 (Fig. 34). The first substrate is thinned from its back surface by a method of grinding or the like, to expose the porous Si 242 across the entire surface of substrate (Fig. 35). The porous Si 242 thus exposed is removed by etching with a selective etchant such as KOH or HF + H_2O_2 (Fig. 36). At this time, the etch selectivity of porous Si to bulk Si

(non-porous single-crystal Si) is sufficiently high, about 100,000. Hence, the non-porous single-crystal Si layer preliminarily grown on the porous layer can be left on the second substrate with little reduction of film thickness thereof, thus forming the SOI substrate. Therefore, the uniformity of film thickness of SOI is determined almost upon epitaxial growth. Since the epitaxial growth allows use of the CVD system used in the normal semiconductor processes, it realized the uniformity thereof, for example 100 nm ± within 2 %, according to the report of Sato et al. (SSDM 95). Also, the crystallinity of the epitaxial Si layer was reported to be as good as 3. 5 x $10^2/cm^2$.

[0070] Since in the conventional methods the etch selectivity depended on the differences of impurity concentration and the depthwise profile, temperatures of thermal treatments (bonding, epitaxial growth, oxidation, etc.) to expand the concentration distribution were greatly restricted to below approximately 800 °C. On the other hand, in the etching of this method, the etch rate is determined by the difference of structure between porous and bulk, and thus there is little restriction on the temperature of the thermal treatments. It is reported that thermal treatment at about 1180 °C is possible. For example, annealing after bonding is known to enhance the bonding strength between wafers and to decrease the number and size of vacancies (voids) occurring in the bonding interface. In such etching based on the structural difference, particles deposited on porous Si at the etching process, if present, do not affect the uniformity of film thickness.

[0071] However, the semiconductor substrate using bonding always requires two wafers, most of one of which is wastefully removed and discarded by polishing, etching, etc., which would result in wasting the earth's limited resources.

[0072] Accordingly, SOI by bonding, according to the existing methods, has a lot of problems regarding controllability, uniformity, and cost efficiency.

SUMMARY OF THE INVENTION

[0073] The present invention intends to improve further the process disclosed in the above European Patent for producing a semiconductor member.

[0074] The present invention further intends to provide a process for producing economically a semiconductor substrate having a monocrystalline layer or a compound semiconductor monocrystalline layer having excellent crystallinity, large-area and a uniform flat surface on a surface of a monocrystalline substrate, in which the substrate is removed to leave the active semiconductor layer to obtain a monocrystalline layer or a compound semiconductor monocrystalline layer formed on the surface and having few defects.

[0075] The present invention still further intends to provide a process for producing a semiconductor substrate on a transparent substrate (light-transmissive substrate) for obtaining a monocrystalline Si semiconductor layer or a monocrystalline compound semiconductor layer having crystallinity as high as that of a monocrystalline wafer with high productivity, high uniformity, high controllability, and low production cost.

[0076] The present invention still further intends to provide a process for producing a semiconductor substrate useful in place of expensive SOS or SIMOX in the production of a large scale integrated circuit of SOI structure.

[0077] A first embodiment of the process for producing a semiconductor substrate of the present invention comprises the steps of: forming a non-porous monocrystalline semiconductor layer on a porous layer of the first substrate having the porous layer; bonding the nonporous monocrystalline layer onto a second substrate; separating the bonded substrates at the porous layer; removing the

porous layer on the second substrate; and removing the porous layer constituting the first substrate.

[0078] A second embodiment of the process for producing a semiconductor substrate of the present invention comprises the steps of: forming a nonporous monocrystalline semiconductor layer on a porous layer of a first substrate having the porous layer; bonding the nonporous monocrystalline layer onto a second substrate with interposition of an insulative layer; separating the bonded substrates at the porous layer; removing the porous layer on the second substrate; and removing the porous layer constituting the first substrate.

[0079] In the present invention, the lamination-bonded substrates are separated at the porous layer, and the porous layer is removed from the second substrate having a nonporous monocrystalline semiconductor layer. Thereby, a semiconductor substrate is prepared which has nonporous monocrystalline semiconductor layer of high quality. Furthermore, the first substrate can be repeatedly used for producing the semiconductor substrate in the next production cycle by removing the remaining porous layer on the first substrate after the separation of the two substrates. Thereby, the semiconductor substrate can be produced with higher productivity and lower cost.

[0080] The present invention enables preparation of a monocrystalline layer of Si or the like, or a monocrystalline compound semiconductor layer having excellent crystallinity similar to monocrystalline wafers on a substrate including a light-transmissive substrate with advantages in productivity, uniformity, controllability, and production cost.

[0081] The present invention further enables production of a semiconductor substrate which can be a substitute for expensive SOS and SIMOX in the production of large scale integrated circuits of an SOI structure.

[0082] According to the present invention, the combined substrates are separated at the porous layer or layers into two or more substrates, and the one or more separated substrates may be used as a semiconductor substrate after removal of the remaining porous layer, and the other substrate may be used repeatedly in the next production cycle of a semiconductor substrate.

[0083] Further, according to the present invention, two semiconductor substrates can be produced simultaneously by forming porous layers and nonporous monocrystalline layers on the both faces of a substrate, bonding thereto two other substrates, and separating the substrates at the porous layer.

[0084] The present invention has an object to provide a semiconductor substrate and a forming method thereof which can solve the foregoing various problems by superposing a finer porous structure in a porous layer.

[0085] As a result of assiduous efforts made by the present inventors, the following invention has been achieved.

[0086] Specifically, a semiconductor substrate of the present invention is characterized by having a porous Si layer at a surface layer of a Si substrate, and a porous Si layer with large porosity existing in a region of the above-mentioned porous Si layer, which region is at a specific depth from the surface of the above-mentioned porous Si layer. In the semiconductor substrate, a non-porous Si portion may exist on the surface of the porous Si layer and an electrode may be formed on respective surfaces of the Si substrate and the nonporous Si layer, so that the semiconductor substrate constitutes a luminescent element.

[0087] According to a semiconductor substrate of the present invention, for example, a structure can be easily achieved, wherein a porous layer having a fine structure to work as a luminescent material is sandwiched in a porous layer having a high mechanical strength, such as porous silicon formed on a p^+-Si substrate. Although the porous layer having such a fine structure differs from bulk Si in lattice constant, by sandwiching it in the large porous Si layer having an intermediate lattice constant, stresses can be relaxed and introduction of cracks or defects can be suppressed. Specifically, since the luminescent layer which can stable in structure can be formed, it not only serves to form peripheral circuit or wiring, but it is also possible to provide a material which is excellent in long-term stability.

[0088] Further, according to a semiconductor substrate of the present invention, an extremely thin porous layer corresponding to a projection range of ion implantation can be formed. Since the pore size of such a porous layer can be set small, that is, no greater than several tens of nanometers, even the small foreign matter contained in gas and exceeding several tens of nanometers in diameter can be removed. Further, a thickness of such a porous layer can be set small, that is, no greater than 20μm, the conductance of the gas can be ensured. Specifically, when using it as a filter for particles in the gas, it is possible to produce a filter which can remove the particles greater than several tens of nanometers in diameter and whose pressure loss is small. Further, if high purity Si which is used in the semiconductor process is used as a substrate, there is no worry about contamination from the filter itself.

[0089] The present invention includes a method of producing a semiconductor substrate.

[0090] Specifically, a method of producing a semiconductor substrate of the present invention comprises a porous-forming step for forming a Si porous substrate and forming a porous Si layer on at least a surface of the Si substrate, and

a high-porosity layer forming step for forming a porous Si layer with large porosity in the region at the specific depth from the porous layer in the porous Si layer. The high-porosity layer forming step can be carried out as an ion implanting step for implanting ions into the porous Si layer with a given projection range. It is preferable that the ions comprise at least one kind of noble gas, hydrogen and nitrogen. It is preferable that a non-porous layer forming step is provided for forming a non-porous layer on a surface of the porous Si layer before the ion implanting step. It is preferable that a bonding step is provided for bonding a support substrate on a surface of the non-porous layer after the high-porosity layer forming step and that a separating step is provided for separating the Si substrate into two at the large porosity porous Si layer after the bonding step. It is preferable that the separating step is performed by heat-treating the Si substrate, by pressurizing the Si substrate in a direction perpendicular to a surface thereof, by drawing the Si substrate in a direction perpendicular to a surface thereof or by applying a shearing force to the Si substrate.

[0091] It is preferable that the non-porous layer is made of single-crystal Si, single-crystal Si having an oxidized Si layer on a surface to be bonded or a single-crystal compound semiconductor. It is preferable that the support substrate is a Si substrate, a Si substrate having an oxidized Si layer on a surface to be bonded or a light transmittable substrate. It is preferable that the bonding step is performed by anode bonding, pressurization, heat treatment or a combination thereof. It is preferable that a porous Si removing step is provided, after the separating step, for removing the porous Si layer exposed on a surface of the support substrate and exposing the non-porous layer. It is preferable that the porous Si removing step is performed by an electroless wet etching using at least one of hydrofluoric acid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding a least one of alcohol and hydrogen peroxide water to buffered hydrofluoric acid. It is preferable that a flattening step

is provided for flattening a surface of the non-porous layer after the porous Si removing step. It is preferable that the flattening step is performed by heat treatment in an atmosphere including hydrogen.

[0092] The porous-forming step may form porous Si layers on both sides of the Si substrate, and the bonding step may bond two support substrates to the porous Si layers formed on both sides of the Si substrate. A second non-porous layer forming step can be provided, after the separating step, for again forming a non-porous layer on the surface of the porous Si layer exposed on the surface of the Si substrate, and that a second ion implanting step is provided, after the porous layer forming step, for implanting ions into the porous Si layer with a given projection range and forming a porous Si layer with large porosity in the porous Si layer. It is preferable that the porous-forming step is performed by anodization. It is preferable that the anodization is performed in a HF solution.

[0093] The high-porosity layer forming step can be carried out by also altering the current density, during the porous-forming step.

[0094] After removing any remaining porous layer, the Si substrate separated by the foregoing method may be reused as a Si substrate by performing the surface flattening process if the surface flatness is insufficient. The surface flattening process may be polishing, etching or the like normally used in semiconductor processing. On the other hand, heat treatment in an atmosphere including hydrogen may also be used. By selecting the conditions, this heat treatment can achieve flatness to an extent where the atomic step is locally presented.

[0095] According to the method of producing the semiconductor substrate of the present invention, upon removal of the Si substrate, the Si substrate can be separated at one time in a large area via the porous layer. Thus, the process can be shortened. Further, since the separating position is limited to within the porous

layer with large porosity due to the ion implantation, thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with excellent selectivity.

[0096] According to the producing method of the semiconductor substrate of the present invention, the Si substrate can be separated in advance in one step over a large area via the porous layer. Thus, the grinding, polishing or etching process which was essential in the prior art for removing the Si substrate to expose the porous silicon layer can be omitted to shorten the process. Further, since the separating position is limited to within the porous layer with large porosity by implanting ions of at least one kind of noble gas, hydrogen and nitrogen into the porous layer so as to have the projection range, thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with excellent selectivity. It is unlikely that the thickness of the remaining porous layer is thin locally, so that the non-porous layer appears on the surface earlier and is etched accordingly. In that case, the method of forming the porous layer having a high porosity is not restricted to ion implantation, but formation can also be realized by altering the electric current at anodization. Specifically, not only the grinding or etching process which was essential in the prior art for exposing porous silicon can be omitted, but also the removed Si substrate can be reused as a Si substrate by removing the remaining porous layer. If the surface flatness after removing the porous silicon is insufficient, the surface flattening process is performed. Since the position where the bonded two substrates are separated is regulated by the projection range, the dispersion of the separating positions within porous silicon does not occur as in the prior art. Thus, upon removal of porous silicon, the single-crystal silicon layer is prevented from being exposed and etched to deteriorate the uniformity of thickness. Further, the Si substrate can be reused in the desired number of times until its structural strength makes it impossible. Further, since the separating position is restricted to around the depth corresponding to the projection range of the ion implantation, the

thickness of the porous layer can be set smaller as compared with the prior art. Further, it is capable of making the layer having a high porosity a layer having a specific depth constant from the surface of the porous layer to separate it, so that the crystallizability of the porous layer is not deteriorated.

[0097] Alternatively, without removing the remaining porous layer, the separated Si substrate can be reused again as a Si substrate of the present invention by forming a non-porous single-crystal Si layer. Also in this case, the Si substrate can be reused in the desired number of times until its structural strength makes it impossible.

[0098] In the conventional method of producing the bonded substrates, the Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the Si substrate is held in the initial state other than its surface layers so that, by using both sides of the Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one Si substrate. Thus, the process can be shortened and the productivity can be improved. As appreciated, also in this case, the separated Si substrate can be recycled as a Si substrate after removing the remaining porous Si.

[0099] Specifically, the present invention uses a single-crystal Si substrate which is economical, flat and uniform over a large area and has excellent crystalline properties, and removes from one side thereof to a Si or compound semiconductor active layer formed on the surface which thus remains, so as to provide a single-crystal Si layer or a compound semiconductor single-crystal layer with fewer defects on an insulating material.

[0100] The present invention provides a method of producing a semiconductor substrate which is capable of achieving a Si or compound semiconductor single-crystal layer with a crystalline property as good as a single-crystal wafer on a transparent substrate (light transmittable substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

[0101] Further, the present invention provides a method of producing a semiconductor substrate which is replaceable for an expensive SOS or SIMOX upon producing a large scale integrated circuit of an SOI structure.

[0102] According to the present invention, the single-crystal compound semiconductor layer with excellent crystalline property can be formed on porous Si, and further, this semiconductor layer can be transferred onto the large-area insulating substrate which is cost efficient. Thus, the foregoing problem of the difference in lattice constant and thermal expansion coefficient can be sufficiently suppressed so as to form the compound semiconductor layer with excellent crystallinity on the insulating substrate.

[0103] Further, since porous Si has a low mechanical strength and an extensive surface area, removing the porous Si layer of the present invention can also be performed by selective polishing using the single-crystal layer as a polishing stopper.

[0104] According to the method of producing the semiconductor substrate, since the porous layer of fine structure can be formed after formation of the single-crystal silicon layer on the porous layer, the epitaxial growth conditions of the single-crystal layer can be free of influence of the structural changes of the porous layer. Specifically, since the fine-structure porous layer, working as a luminescent layer, which tends to change due to thermal treatment, can be formed

after completion of thermal treatment for the film formation, its characteristics can be stable.

[0105] According to the method of producing the semiconductor substrate, upon removing the Si substrate, the Si substrate can be separated in one step over a large area via the porous layer and, the process can be shortened. Further, since the separating position is limited to within the porous layer by means of the ion implantation, thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with high selectivity. Thus, even when etching is unstable due to the size of apparatus or the change of the environment, the non-porous thin film, such as the single-crystal Si layer or the compound semiconductor single-crystal layer, which is economical, flat and uniform over the large area and has the extremely excellent crystalline property, can be transferred onto the support substrate with high yield. Specifically, the SOI structure with the single-crystal Si layer formed on the insulating layer can be obtained with high uniformity of film thickness and high yield. Further, since the separating position is regulated by the project range of the ion implantation so as to be within the porous layer, the thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with high selectivity. Further, the removed Si substrate can be reused as an Si substrate by removing the remaining porous layer. If the surface flatness after removing porous silicon is insufficient, the surface flattening process is performed.

[0106] The present invention provides a producing method of a semiconductor substrate which is capable of achieving a Si or compound semiconductor single-crystal layer with a crystalline property as good as a single-crystal wafer on a transparent substrate (light transmittable substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

[0107] According to the method of producing the semiconductor substrate of the present invention, since the selective etching with a good ratio of etching selectively can be performed, by performing the bonding with the support substrate, a SOI substrate or the compound semiconductor single crystal on the support substrate, which is flat and uniform over the large area and has an extremely excellent crystalline property, can be achieved.

[0108] Further, according to the method of producing the semiconductor substrate, the single-crystal compound semiconductor layer with high crystalline property can be formed on porous Si, and further, this semiconductor layer can be transferred onto a large-area insulating substrate which is economical. Thus, the foregoing problems of the differences in lattice constants and thermal expansion coefficients can be sufficiently suppressed to form the compound semiconductor layer with excellent crystalline properties on the insulating substrate.

[0109] Further, even if non-formation regions of the implanted layer are formed due to presence of foreign matter on the surface upon ion implantation, since the mechanical strength of the porous layer itself is smaller than bulk Si, the separation occurs in the porous layer. Thus, the two bonded substrates can be separated without causing damages such as cracks in the non-porous single-crystal silicon layer.

[0110] Further, since the gettering effect is available at the ion-implanted region, even if metal impurities exist, the two bonded substrates are separated after achieving the gettering of the impurities into the ion-implanted region, and then the ion-implanted region is removed so that it is also effective against impurity contamination.

[0111] Further, since the separating region is limited to the ion-implanted region within the porous layer, the depths of the separating region do not disperse within

the porous layer. Accordingly, even if the ratio of selectively etching porous silicon is insufficient, a time for removing porous silicon can be rendered substantially constant so that the thickness uniformity of the single-crystal silicon layer transferred onto the support substrate is not spoiled.

[0112] The inventor has made strenuous efforts to achieve the above object and obtain the following invention. Namely, a first fabrication process for a semiconductor substrate according to the present invention is a fabrication process comprising: a step of bonding a principal surface of a first substrate to a principal surface of a second substrate, the first substrate being an Si substrate in which at least one layer of non-porous thin film is formed through a porous Si layer; a step of exposing the porous Si layer in a side surface of a bonding substrate comprised of the first substrate and the second substrate; a step of dividing the bonding substrate in the porous Si layer by oxidizing the bonding substrate; and a step of removing a porous Si and oxidized porous Si layer on the second substrate separated by the division of the bonding substrate in the porous Si layer.

[0113] Further, a second fabrication process for a semiconductor substrate according to the present invention is a fabrication process comprising: a step of bonding a principal surface of a first substrate to a principal surface of a second substrate, the first substrate being a Si substrate in which at least one layer of non-porous thin film is formed through a porous Si layer and in which the porous Si layer is exposed in a side surface thereof; a step of dividing the bonding substrate in the porous Si layer by oxidizing a bonding substrate comprised of the first substrate and the second substrate; and a step of removing a porous Si and oxidized porous Si layer on the second substrate separated by the division of the bonding substrate in the porous Si layer.

[0114] Also, a third fabrication process for a semiconductor substrate according to the present invention is one according to the above first or second fabrication,

wherein after removing the porous Si and oxidized porous Si layer on the first substrate separated by the division of the bonding substrate in the porous Si layer, the first substrate is again used as a raw material for the first substrate before bonding.

[0115] In addition, a fourth fabrication process for a semiconductor substrate according to the present invention is one according to the above first or second fabrication process, wherein after removing the porous Si and oxidized porous Si layer on the first substrate separated by the division of the bonding substrate in the porous Si layer, the first substrate is again used as a raw material for the second substrate before bonding.

[0116] Moreover, a fifth fabrication process for a semiconductor substrate according to the present invention is one according to any of the above first to fourth fabrication processes, wherein at least one layer of non-porous thin film is formed through a porous Si layer on each of two principal surfaces of the first substrate and the second substrate is bonded to each of the two principal surfaces.

[0117] The present invention utilizes enhanced oxidation of porous Si to oxidize the porous Si layer from the periphery of the wafer, whereby volume expansion of porous Si becomes greater from the center to the periphery. This seems as if porous Si is uniformly wedged from the periphery, so that the internal pressure is exerted on only the porous layer, and it splits the wafer in the porous Si layer therethrough across the entire surface of the wafer. This provides a fabrication process for a semiconductor substrate solving the various problems discussed above.

[0118] Namely, in the case of the bonding substrate having a multi-layered structure, if the method of splitting at porous Si by external pressure is applied and if the substrate has an interface with low strength or a partially weak region, the

substrate will be split at the weak portion. In contrast, the present invention permits the internal pressure to be exerted only on the porous Si layer by utilizing oxidation, one step of the normal Si-IC processes, excellent in uniformity, and by combining high-speed oxidizability of porous Si, volume expansion of porous Si, and fragility of porous Si, whereby the wafer can be split with good controllability in and through the porous Si layer.

[0119] Further, use of the process according to the present invention enables reuse of the first Si substrate after removal of the porous substrate portion. This first Si substrate can be reused any number of times before it becomes unusable with respect to its mechanical strength.

[0120] The present invention permits separation through the porous layer over a large area in removing the first Si substrate. The first Si substrate thus removed can be reused again as a first Si substrate or as a next second substrate after removing the residual porous layer or after flattening the surface if the surface is too rough. The surface flattening process may be polishing, etching, or any other method used in the normal semiconductor processes, but may be annealing in an atmosphere containing hydrogen. By selecting suitable conditions for this annealing, the surface can be flattened so as to reveal atomic steps locally. In the case of repetitive use as a first Si substrate, this first Si substrate can be reused any number of times before it becomes unusable with respect to its mechanical strength.

[0121] Since the present invention permits division of a large area en bloc through the porous layer, it can obviate the need for the grinding, polishing, and etching steps conventionally essential for removing the first substrate to expose the porous Si layer, thereby decreasing the steps. In addition, the position of division can be defined at a limited depth in the porous Si layer by preliminarily performing ion implantation of at least one element chosen from rare gases, hydrogen, and

nitrogen so as to have the projected range in the porous layer, which evens the thickness of the porous layer remaining on the second substrate side. Then the porous layer can be removed uniformly even with an etchant having low to moderate etch selectivity. Further, the conventional fabrication of a bonding substrate employed a method for successively removing the first Si layer from one surface by grinding and etching, therefore making it impossible to bond the two surfaces of the first Si layer with respective support substrates, thereby effectively utilizing both surfaces. In contrast, according to the present invention, the first Si substrate, except for the surface layer thereof, is maintained as it was, and two substrates can be fabricated simultaneously by bonding, dividing and thinning, with the aid of a first Si substrate by using both surfaces of the first Si substrate as principal surfaces and bonding support substrates to the respective surfaces, thereby raising productivity. Of course, the first Si substrate after division can be reused.

[0122] In addition, the present invention permits a large area to be divided en bloc through the porous layer in removing the first Si substrate. This method decreases processing steps, which is economically desirable, and can transfer a non-porous thin film such as a Si single-crystal layer or a compound semiconductor single-crystal layer, which is uniformly flat across a large area and which has excellent crystallinity, to the second substrate at a good yield. Namely, the SOI structure with the Si single-crystal layer formed on the insulating layer can be attained with good uniformity of film thickness and at a good yield.

[0123] In other words, the present invention provides the Si single-crystal layer or the compound semiconductor single-crystal layer with a remarkably reduced number of imperfections on the insulator by using a Si single-crystal substrate in an economically desirable amount, which exhibits uniform flatness across a large area and excellent crystallinity, by removing the portion from its one surface to the

active layer and leaving the Si or compound semiconductor active layer formed on the surface.

[0124] The present invention provides a fabrication process for a semiconductor substrate superior with respect to productivity, uniformity, controllability, and cost in obtaining the Si or compound semiconductor single-crystal layer with excellent crystallinity equivalent to that of a single-crystal wafer, on a transparent substrate (light transmissive substrate).

[0125] The fabrication process for a semiconductor substrate according to the present invention involves performing selective etching with outstandingly excellent etch selectivity, thereby enabling one to obtain a Si single crystal or compound semiconductor single crystal which is uniformly flat across a large area and which has excellent crystallinity.

[0126] Further, removal of the porous Si layer of the present invention can also be done by selective polishing, using the single-crystal layer as a polishing stopper because porous Si has low mechanical strength and enormous surface area.

[0127] Also, the present invention can provide a fabrication process for a semiconductor substrate that can replace the expensive SOS or SIMOX for fabricating large-scale integrated circuits of the SOI structure.

[0128] The present invention can form a single-crystal compound semiconductor layer with good crystallinity on porous Si, can transfer the semiconductor layer onto an economically desirable and large-area insulating substrate, and can form the compound semiconductor layer with good crystallinity on the insulating substrate while restraining the differences in lattice constant and coefficient of thermal expansion, which were problems in the prior art.

[0129] In the present invention, a layer of a material having a smaller coefficient of thermal expansion than that of Si is formed at least on one side of the outer surfaces of the bonding substrate before splitting by oxidation (or possibly before bonding), whereby at temperatures during oxidation, Si becomes more likely to expand and thus stress acts in the wafer peeling directions in the peripheral region of the bonding wafer, facilitating occurrence of the wedge effect by oxidation.

[0130] Also, in the case where regions without an implant layer are formed due to the existence of contaminations on the surface upon ion implantation, because the mechanical strength of the porous layer itself is smaller than that of bulk Si, peeling occurs in the porous layer, so that the two substrates bonded can be divided without extending damages such as cracks to the non-porous single-crystal Si layer.

[0131] Since the ion implant region has the gettering effect, metal impurities, if present, can be subject to gettering by the ion implant region and thereafter the ion implant region with the impurities can be removed by separating the two substrates bonded. It is thus effective with respect to impurity contamination.

[0132] The present invention may combine anodization with ion implantation to make the porosity of the side surface small and the porosity of the central part large, thereby making the volume expansion of the side surface greater and the strength of the central part low so as to facilitate peeling.

BRIEF DESCRIPTION OF THE DRAWINGS

[0133] Figs. 1A to 1E are schematic drawings for explaining an example of the process of the present invention.

[0134] Figs. 2A to 2E are schematic drawings for explaining another example of the process of the present invention.

[0135] Figs. 3A to 3E are schematic drawings for explaining still another example of the process of the present invention.

[0136] Figs. 4A to 4E are schematic drawings for explaining a further example of the process of the present invention.

[0137] Figs. 5A to 5E are schematic drawings for explaining a still further example of the process of the present invention.

[0138] Figs. 6A to 6E are schematic diagrams for explaining a conventional semiconductor substrate producing process;

[0139] Figs. 7A and 7B are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 6 of the present invention;

[0140] Figs. 8A to 8C are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 7 of the present invention;

[0141] Figs. 9A to 9C are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 8 of the present invention;

[0142] Figs. 10A to 10D are sectional views showing a process of an EL element;

[0143] Figs. 11A to 11F are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 9 of the present invention;

[0144] Figs. 12A to 12F are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 10 of the present invention;

[0145] Figs. 13A to 13E are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 11 of the present invention;

[0146] Figs. 14A and 14B are schematic diagrams for explaining anodization;

[0147] Figs. 15A to 15G are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 12 of the present invention;

[0148] Figs. l6A to l6G are schematic diagrams for explaining a semiconductor substrate producing process according to a preferred embodiment 13 of the present invention;

[0149] Fig. 17 is a schematic cross-sectional view for explaining a step of another example;

[0150] Fig. 18 is a schematic cross-sectional view for explaining a step of another example;

[0151] Fig. 19 is a schematic cross-sectional view for explaining a step of another example;

[0152] Fig. 20 is a schematic cross-sectional view for explaining the principle of the present invention;

[0153] Fig. 21 is a schematic cross-sectional view for explaining the principle of the present invention;

[0154] Fig. 22 is a schematic cross-sectional view for explaining the principle of the present invention;

[0155] Fig. 23 is a schematic cross-sectional view for explaining a step of the present invention;

[0156] Fig. 24 is a schematic cross-sectional view for explaining a step of the present invention;

[0157] Fig. 25 is a schematic cross-sectional view for explaining a step of the present invention;

[0158] Fig. 26 is a schematic cross-sectional view for explaining a step of the present invention;

[0159] Fig. 27 is a schematic cross-sectional view for explaining a step of the present invention;

[0160] Fig. 28 is a schematic cross-sectional view for explaining a step of the present invention;

[0161] Fig. 29 is a schematic cross-sectional view for explaining a step of the present invention;

[0162] Fig. 30 is a schematic cross-sectional view for explaining a step of the present invention;

[0163] Fig. 31 is a schematic cross-sectional view for explaining a step of the present invention;

[0164] Fig. 32 is a schematic cross-sectional view for explaining a step of the present invention;

[0165] Figs. 33A to 33E are schematic diagrams for explaining a semiconductor substrate producing process which has been proposed before;

[0166] Fig. 34 is a schematic cross-sectional view for explaining a step of the conventional example;

[0167] Fig. 35 is a schematic cross-sectional view for explaining a step of the conventional example; and

[0168] Fig. 36 is a schematic cross-sectional view for explaining a step of the conventional example.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0169] The process for producing a semiconductor substrate of the present invention is described by employing a silicon substrate as an example.

[0170] The mechanical strength of porous silicon is much lower than that of bulk silicon depending on the porosity thereof. For instance, porous silicon having a porosity of 50% is considered to have half the mechanical strength of bulk silicon.

Therefore, on application of a tensile force, a compressive force, or a shearing force to a laminated wafer, the porous layer will be broken first. The larger the porosity of the porous layer, the less force is needed for the breakdown of the layer.

[0171] A silicon substrate can be made porous by anodization in an HF solution. The resulting porous Si layer has a density ranging from 1.1 to 0.6 g/cm^3 depending on the HF solution concentration of from 50 to 20% in comparison with the density of 2.33 g/cm^3 of monocrystalline Si. The porous layer is formed only on a P-type Si substrate, but is not formed on an N-type Si layer for the reasons described later. The porous Si layer has pores of about 600 Å in average diameter according to transmissive electron microscopy.

[0172] The porous Si was found by Uhlir, et al. in the year 1956 during the study of electropolishing of semiconductors (A. Uhlir: Bell Syst. Tech. J., vol. 35, p. 333 (1956)).

[0173] Unagami, et al. found that positive holes are required for anodization of Si in an HF solution, and the reactions proceed as shown in their report on dissolution of Si in anodization (T. Unagami, et al.: J. Electrochem. Soc., vol. 127, p. 476 (1980)) as below:

$$Si + 2HF + (2-n)e^+ \rightarrow SiF_2 + 2H^+ + ne^-$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (2-\lambda)e^+ \rightarrow SiF_4 + 4H^+ + \lambda e^-$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

where e^+ and e^- represent respectively a positive hole and an electron; n and λ represent respectively the number of positive holes required for dissolving one Si

atom. Unagami reported that porous Si is formed under the condition of $n > 2$, or $\lambda > 4$.

[0174] According to the above consideration, P-type Si which has positive holes can be made porous, whereas N-type Si cannot be made porous. This selectivity .for porosity was evidenced by Nagano, et-al., and Imai (Nagano, Nakajima, Yasuno, Oonaka, and Kajihara: Denshi Tsushin Gakkai Gijutsu Kenkyu Hokoku (Technical Research Report of Electronic communication society) vol. 79, SSD79-9549 (1979); and K. Imai: Solid-State Electronics, vol. 24, p. 159 (1981)).

[0175] On the other hand, a report is found that high concentration N-type Si can be made porous (R.P. Holmstrom and J.Y. Chi: Appl. Phys. Lett., Vol. 42, p. 386 (1983)). Therefore, selection'of the substrate is important for producing porous Si regardless of P-type or N-type.

[0176] The porous Si layer has pores of about 600 Å in average diameter by observation by transmission electron microscopy, and the density is less than half that of monocrystalline Si. Nevertheless, the single crystallinity is maintained, and thereon a monocrystalline Sican be made to grow epitaxially in layer. However, in the epitaxal growth at a temperature of 1000°C or higher, the internal pores will come to be rearranged, which impairs the accelerated etching characteristics. Therefore, low temperature growth processes are preferred for epitaxial growth of the Si layer, such as molecular beam epitaxial growth, plasma CVD, reduced pressure CVD, photo-assisted CVD, bias sputtering, and liquid-phase epitaxial growth.

[0177] The porous layer has a large volume of voids therein, having a half or lower density of the material, and having a surface area remarkably large for the volume. Accordingly, the chemical etching is greatly accelerated in comparison with that of the normal monocrystalline layer.

Embodiment 1

[0178] A first monocrystalline Si substrate 11 is made porous at the surface to form a porous layer 12 as shown in Fig. 1A. Then, nonporous monocrystalline Si layer 13 is formed on the porous Si layer 12 as shown in Fig. 1B.

[0179] Another Si supporting substrate 14 is brought into contact with the nonporous monocrystalline Si layer 13 with interposition of an insulative layer 15 at room temperature as shown in Fig. 1C, and then the contacted matter was subjected to anode coupling, compression, heat treatment, or combination thereof to bond tightly the Si supporting substrate 14 and the monocrystalline layer 13 with interposition of the insulative layer 15. The insulative layer 15 may be formed preliminarily on either one of the monocrystalline Si layer 13 or the Si supporting substrate 14, or the three sheets may be bonded with an insulative thin film interposed.

[0180] Subsequently, the substrates are separated at the porous Si layer 12 as shown in Fig. 1D. On the Si supporting substrate 14, the layers have the structure of porous Si 12 / monocrystalline Si layer 13 / insulative layer 15 / Si supporting substrate 14.

[0181] The porous Si 12 is removed selectively by nonelectrolytic wet chemical etching by use of at least one of a usual Si etching solution, hydrofluoric acid or a mixture of hydrofluoric acid with alcohol and/or hydrogen peroxide as the porous Si-selective etching solution, and buffered hydrofluoric acid or a mixture of hydrofluoric acid with alcohol and/or hydrogen peroxide to leave the thin-layered monocrystalline Si layer 13 on the insulative substrate 15 and 14. As described above in detail, the porous Si can be etched selectively by a usual Si etching solution owing to the extremely large surface area of the porous surface area.

[0182] Otherwise, the porous Si 12 is selectively removed by grinding by utilizing the monocrystalline Si layer 13 as the grinding stopper.

[0183] Fig. 1E illustrates a semiconductor substrate of the present invention. The monocrystalline Si layer 13 is formed flat and uniformly in a thin layer on the insulative substrate 15 and 14 over the entire large area of the wafer. The resulting semiconductor substrate is useful for production of insulation-isolated electronic elements.

[0184] The first monocrystalline Si substrate 11 may be repeatedly used for the same use after removal of the remaining Si and surface flattening treatment if the surface has become roughened unacceptably in the next production cycle.

[0185] The method of separation of the two substrates at the porous Si layer in the present invention includes crushing of the porous layer by compression on both faces of the bonded substrates; pulling of the respective substrates in opposite directions; insertion of a jig or the like into the porous layer; application of force in opposite directions parallel to the bonded face of the substrates; application of supersonic vibration to the porous layer; and so forth.

[0186] The porosity of the porous Si layer suitable for the separation ranges generally from 10 to 80%, preferably from 20 to 60%.

Embodiment 2

[0187] A first monocrystalline Si substrate 21 is made porous at the surface to form a porous layer 22 as shown in Fig. 2A. Then a nonporous monocrystalline Si layer 23 is formed on the porous Si layer 22 as shown in Fig. 2B.

[0188] A light-transmissive supporting substrate 24 is brought into contact with the monocrystalline Si layer 23 with interposition of an insulative layer 25 at room temperature as shown in Fig. 2C, and then the contacted matter was subjected to anode coupling, compression, heat treatment, or combination of the treatment to bond tightly the light-transmissive supporting substrate 24 and the monocrystalline layer 23 with interposition of the insulative layer 25. The insulative layer 25 may be formed preliminarily on either one of the monocrystalline Si layer or the light-transmissive supporting substrate 24, or the three sheets may be bonded with interposition of an insulative thin film.

[0189] Subsequently, the substrates are separated at the porous Si layer 22 as shown in Fig. 2D. On the light-transmissive supporting substrate, the layers have the structure of porous Si 22 / monocrystalline Si layer 23 / insulative layer 25 / light-transmissive supporting substrate 24.

[0190] The porous Si 22 is removed selectively by non-electrolytic wet chemical etching by use of at least one of a usual Si etching solution, hydrofluoric acid or a mixture of hydrofluoric acid with alcohol and/or hydrogen peroxide as the porous Si-selective etching solution, and buffered hydrofluoric acid or a mixture of hydrofluoric acid with alcohol and/or hydrogen peroxide to leave a thin-layered monocrystalline Si layer 23 on the insulative substrate 25 and 24. As described above in detail, the porous Si can be etched selectively by a usual Si etching solution because of the extremely large surface area of the porous surface area.

[0191] Otherwise, the porous Si 23 is selectively removed by grinding by utilizing the monocrystalline Si layer 22 as the grinding stopper.

[0192] Fig. 2E illustrates a semiconductor substrate of the present invention. The monocrystalline Si layer 23 is formed flat and uniformly in a thin layer on the insulative substrate 25 and 24 over the entire large area of the wafer. The obtained

semiconductor substrate is useful for production of insulation-isolated electronic elements.

[0193] The presence of the interposed insulative layer 25 is not essential.

[0194] The first monocrystalline Si substrate 21 may be repeatedly used for the same use after removal of the remaining Si and surface flattening treatment if the surface has become roughened unacceptably in the next production cycle.

Embodiment 3

[0195] A first monocrystalline Si substrate 31 is made porous at the surface to form a porous layer 32 as shown in Fig. 3A. Then a nonporous monocrystalline compound semiconductor layer 33 is formed on the porous Si layer 32 as shown in Fig. 3B.

[0196] Another Si supporting substrate 34 is brought into close contact with the monocrystalline compound semiconductor layer 33 with interposition of an insulative layer 35 at room temperature as shown in Fig. 3C, and then the contacted matter was subjected to anode coupling, compression, or heat treatment, or combination of the treatments to bond tightly the Si supporting substrate 34 and the monocrystalline layer 33 with interposition of the insulative layer 35. The insulative layer 35 may be formed preliminarily on either one of the monocrystalline compound semiconductor layer or the Si supporting substrate 34, or the three sheets may be bonded with interposition of an insulative thin film.

[0197] Subsequently, the substrates are separated at the porous Si layer 32 as shown in Fig. 3D. On the Si supporting substrate, the layers have the structure of porous Si 3 2 / monocrystalline compound semiconductor layer 33 / insulative layer 35 / Si supporting substrate 34.

[0198] The porous Si 32 is removed selectively by chemical etching by use of an etching solution which is capable of etching Si at a higher etching rate than the compound semiconductor to leave the thin-layered monocrystalline compound semiconductor layer 33 on the insulative substrate 35 and 34.

[0199] Otherwise, the porous Si 32 is selectively removed by grinding by utilizing the monocrystalline compound semiconductor layer 33 as the grinding stopper.

[0200] Fig. 3E illustrates a semiconductor substrate of the present invention. The monocrystalline compound semiconductor layer 33 is formed flat and uniformly in a thin layer on the insulative substrate 35 and 34 over the entire large area of the wafer. The resulting semiconductor substrate is useful as a compound semiconductor substrate and for production of insulation-isolated electronic elements.

[0201] When the substrate is used as a compound semiconductor substrate, the insulative layer 35 is not essential.

[0202] The first monocrystalline Si substrate 31 may be repeatedly used for the same use after removal of the remaining Si and surface flattening treatment if the surface has become roughened unacceptably in the next production cycle.

Embodiment 4

[0203] A first monocrystalline Si substrate 41 is made porous at the surface to form a porous layer 42 as shown in Fig. 4A. Then a nonporous monocrystalline compound semiconductor layer 43 is formed on the porous Si layer 42 as shown in Fig. 4B.

[0204] A light-transmissive supporting substrate 44 is brought into close contact with the monocrystalline compound semiconductor layer 43 with interposition of an insulative layer 45 at room temperature as shown in Fig. 4C, and then the contacted matter was subjected to anode coupling, compression, heat treatment, or combination of the treatments to bond tightly the light-transmissive supporting substrate 44 with the monocrystalline layer 43 with interposition of the insulative layer 45. The insulative layer 45 may be formed preliminarily on either one of the monocrystalline compound semiconductor layer or the light-transmissive supporting substrate 44, or the three sheets may be bonded with interposition of an insulative thin film.

[0205] Subsequently, the substrates are separated at the porous Si layer 42 as shown in Fig. 4D. On the light-transmissive supporting substrate, the layers have the structure of porous Si 42 / monocrystalline compound semiconductor layer 43 / insulative layer 45 / light-transmissive supporting substrate 44.

[0206] The porous Si 42 is removed selectively by chemical etching by use of an etching solution which is capable of etching Si at a higher etching rate than the compound semiconductor to leave a thin-layered monocrystalline compound semiconductor layer 43 on the insulative substrate 45 and 44.

[0207] Otherwise, the porous Si 42 is selectively removed by grinding by utilizing the monocrystalline compound semiconductor layer 43 as the grinding stopper.

[0208] Fig. 4E illustrates a semiconductor substrate of the present invention. The monocrystalline compound semiconductor layer 43 is formed flat and uniformly in a thin layer on the insulative substrate 45 and 44 over the entire large area of the wafer. The resulting semiconductor substrate is useful for production of insulation-isolated electronic elements.

[0209] The insulative layer 45 is not essential in this embodiment.

[0210] The first monocrystalline Si substrate 41 may be repeatedly used for the same use after removal of the remaining Si and surface flattening treatment if the surface has become roughened unacceptably in the next production cycle.

Embodiment 5

[0211] A first monocrystalline Si substrate 51 is made porous at the both faces to form porous layers 52, 53 as shown in Fig. 5A. Then, nonporous monocrystalline compound semiconductor layers 54, 55 are formed on the porous Si layers 52, 53 as shown in Fig. 5B.

[0212] Two supporting substrates 56, 57 are brought into close contact with the monocrystalline semiconductor layers 54, 55 with interposition of insulative layers 58, 59 respectively at room temperature as shown in Fig. 5C, and then the contacted matter is subjected to anode coupling, compression, heat treatment, or combination of the treatments to bond tightly the supporting substrates 56, 57 and the monocrystalline layers 54, 55 with interposition of the insulative layers 58, 59. In the bonding, the respective insulative layers 58, 59 may be formed preliminarily on either one of the monocrystalline semiconductor layer 54, 55 or the supporting substrate 56, or the five sheets may be bonded with interposition of insulative thin films.

[0213] Subsequently, the substrates are separated into three at the both porous Si layers 52, 53 as shown in Fig. 5D. The two supporting substrates come to have a structure of porous Si / monocrystalline semiconductor layer / insulative layer / supporting substrate (52/54/58/56, and 53/55/59/57).

[0214] The porous Si layers 52, 53 are removed selectively by chemical etching to leave thin-layered monocrystalline semiconductor layers 54, 55 on the supporting substrates 58/56 and 59/57.

[0215] Otherwise, the porous Si 52, 53 is selectively removed by grinding by utilizing the monocrystalline semiconductor layers 54, 55 as the grinding stopper.

[0216] Fig. 5E illustrates semiconductor substrates prepared according to the present invention. The monocrystalline compound semiconductor layers are formed flat and uniformly in a thin layer on the supporting substrates over the entire large area of the two wafers at a time with a large area. The resulting semiconductor substrate is useful for production of insulation-isolated electronic elements.

[0217] The insulative intervening layers 58, 59 are not essential.

[0218] The supporting substrates 56, 57 need not be the same.

[0219] The first monocrystalline Si substrate 51 may be repeatedly used for the same use after removal of the remaining Si and surface flattening treatment if the surface has become roughened unacceptably in the next production cycle.

Example 1

[0220] A first monocrystalline (100) Si substrate of P-type having a diameter of 6 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions as below:

Current density:	5 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	12 minutes

Thickness of porous Si:	10 μm
Porosity:	15 %

[0221] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si, monocrystalline Si was allowed to grow epitaxially in a thickness of 1 μm by CVD (chemical vapor deposition) under the growth conditions below:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 ℓ/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0222] The face of the epitaxially grown Si layer was thermally oxidized to form an SiO_2 layer of 100 nm thick.

[0223] On the face of this Si substrate, a separately prepared second Si substrate having an SiO_2 layer of 500 nm thick was superposed with the SiO_2 layer inside, and the superposed matter was heat-treated at 900°C for 2 hours to bond the substrates tightly.

[0224] A pulling force was applied to the resulting bonded wafer in the direction perpendicular to the wafer face in such a manner that a plate was bonded respectively to each of the both faces of the wafer with an adhesive and the plates were pulled to opposite directions with a jig. Consequently, the porous Si layer was broken to cause separation of the wafer into two sheets with the porous Si layers exposed.

[0225] The porous Si layer on the second substrate was etched selectively in a mixture of 49% hydrofluoric acid and 30% hydrogen peroxide (1:5) with agitation. The porous Si was etched and removed completely with the monocrystalline Si remaining unetched as an etching stopper. The etching rate of the nonporous monocrystalline Si was extremely low, the selection ratio of the etching rate of the porous Si being 10^5 or higher. Therefore, the decrease in thickness of the nonporous layer by etching was practicably negligible (several tens of Å).

[0226] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm on an Si oxide film. The monocrystalline Si layer did not change at all by the selective etching of the porous Si layer.

[0227] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0228] Thus an SOI substrate was obtained which has a semiconductor layer of high quality.

[0229] The other Si substrate having been separated at the porous Si layer portion was etched in the same manner as above to remove the remaining porous layer, and its surface was polished. The obtained Si substrate was used repeatedly for the same use in the next production cycle. Thereby a plurality of SOI substrates having a semiconductor layer of high quality were obtained.

Example 2

[0230] A first monocrystalline (100) Si substrate of P-type having a diameter of 4 inches, a thickness of 525 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions as below:

Current density:	7 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	12 minutes
Thickness of porous Si:	10 μm
Porosity:	15 %

[0231] This substrate was oxidized at 400°C in an oxygen atmosphere for 2 hours. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si, monocrystalline Si was allowed to grow epitaxially in a thickness of 0.5 μm by MBE (molecular beam epitaxy) under the growth conditions below:

Temperature:	700°C
Pressure:	1×10^{-9} Torr
Growth rate:	0.1 μm/sec
Temperature:	950°C
Growth rate:	0.3 μm/min

[0232] The face of the epitaxially grown Si layer was thermally oxidized to form an SiO_2 layer of 100 nm thick.

[0233] On the face of the SiO_2 layer, was superposed a separately prepared fused quartz substrate, and the superposed matter was heat-treated at 400°C for 2 hours to bond the substrates.

[0234] A sufficient compression force was applied uniformly to the resulting bonded wafer in the direction perpendicular to the wafer face such that plates were bonded to each of the both faces of the wafer with an adhesive and the compression force was applied with the same jig as in Example 1.

[0235] Consequently, the porous Si layer was broken to cause separation of the wafer into two sheets with the porous Si layers exposed.

[0236] The porous Si layers were etched selectively in a mixture of buffered hydrofluoric acid and 30% hydrogen peroxide (1:5) with agitation. Thereby the porous Si was etched and removed completely with the monocrystalline Si remaining unetched as an etch-stop material. The etching rate of the nonporous monocrystalline Si was extremely low, the selection ratio of the etching rate of the porous Si being, 10^5 or higher. Therefore, the decrease in thickness of the nonporous layer by etching was practicably negligible (several tens of Å).

[0237] Consequently, a monocrystalline Si layer was formed in a thickness of 0.5 μm on a fused quartz substrate. The monocrystalline Si layer did not change at all by the selective etching of the porous Si layer.

[0238] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0239] A plurality of SOI substrates having a semiconductor layer of high quality were prepared by repeating the above process in the same manner as in Example 1.

Example 3

[0240] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 6 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions as below:

Current density:	7 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	12 minutes
Thickness of porous Si:	10 μm
Porosity:	15 %

[0241] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si, monocrystalline GaAs was allowed to grow epitaxially in a thickness of 1 μm by MOCVD (metal organic chemical vapor deposition) under the growth conditions below:

Source gas:	TMG / AsH_3 / H_2
Gas pressure:	80 Torr
Temperature:	700°C

[0242] On the face of the formed GaAs layer, was superposed a separately prepared second Si substrate, and the superposed matter was heat-treated at 900°C for one hour to bond the substrates tightly.

[0243] A sufficient compression force was applied to the resulting bonded wafer in the same manner as in Example 2. Thereby, the porous Si layer was broken to allow the wafer to separate into two sheets with the porous Si layers exposed.

[0244] Then, the oxide film on the inner wall of the porous Si layer was removed by hydrofluoric acid, and the porous Si was etched with a mixture of ethylene diamine, pyrocathecol, and water (17 ml : 3 g : 8 ml) at 110°C. Thereby the porous Si was etched selectively and removed completely with the monocrystalline GaAs remaining unetched as an etch-stopping material. The etching rate of the nonporous monocrystalline GaAs was extremely low and practicably negligible.

[0245] Consequently, a monocrystalline GaAs layer was formed in a thickness of 1 μm on a Si substrate. The monocrystalline GaAs layer did not change at all by the selective etching of the porous Si layer.

[0246] The cross-section of the GaAs layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the GaAs layer and the excellent crystallinity was retained.

[0247] A plurality of semiconductor substrates having a GaAs layer of high quality were prepared by repeating the above process in the same manner as in Example 2.

[0248] GaAs on an insulative film was also prepared by employing an Si substrate having an oxide film as the supporting substrate.

Example 4

[0249] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 5 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions as below:

Current density:	10 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	24 minutes
Thickness of porous Si:	20 μm
Porosity:	17 %

[0250] This substrate was oxidized at 400°C in an oxygen atmosphere for 2 hours. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si, monocrystalline AlGaAs was allowed to grow epitaxially in a thickness of 0..5 μm by MBE (molecular beam epitaxy).

[0251] On the face of the formed AlGaAs layer, was superposed a face of a separately prepared low-melting glass substrate. The superposed matter was heat-treated at 500°C for 2 hours to bond the substrates tightly.

[0252] A sufficient compression force was applied to the resulting bonded wafer in the same manner as in Example 2. Thereby, the porous Si layer was broken to allow the wafer to separate into two sheets with the porous Si layers exposed.

[0253] The porous Si was etched with hydrofluoric acid solution. Thereby the porous Si was etched selectively and removed off completely with the monocrystalline AlGaAs remaining unetched as an etch-stopping material. The etching rate of the nonporous monocrystalline AlGaAs was extremely low and practicably negligible.

[0254] Consequently, a monocrystalline AlGaAs layer was formed in a thickness of 0.5 μm on a glass substrate. The monocrystalline AlGaAs layer did not change at all by the selective etching of the porous Si layer.

[0255] The cross-section of the AlGaAs layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the AlGaAs layer and the excellent crystallinity was retained.

[0256] A plurality of semiconductor substrates having a GaAs layer of high quality were prepared by repeating the above process in the same manner as in Example 2.

Example 5

[0257] A first monocrystalline (100) Si substrate of P-type or N-type having been polished on the both faces and having a diameter of 6 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized on the both faces in an HF solution under the anodization conditions below:

Current density:	5 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	12 x 2 minutes
Thickness of porous Si:	10 μm each
Porosity:	15 %

[0258] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on the both faces of the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 1 μm respectively by CVD (chemical vapor deposition) under the growth conditions below:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 ℓ/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0259] The faces of the formed epitaxial Si layers were thermally oxidized to form SiO_2 layers in a thickness of 100 nm.

[0260] On each of the faces of the SiO_2 layers, a separately prepared Si substrate having a 500-nm thick SiO_2 layer was superposed respectively with the SiO_2 layers

inside, and the superposed matter was heat-treated at 600°C for 2 hours to bond the substrates tightly.

[0261] A sufficient pulling force was applied to the resulting bonded wafer in the direction perpendicular to the bonded wafer face in the same manner as in Example 1. Thereby, the two porous Si layers were broken to allow the wafer to separate into three sheets with the porous Si layers exposed.

[0262] The porous Si layers were etched selectively with a mixture of 49% hydrofluoric acid with 30% hydrogen peroxide (1:5) with agitation. Thereby the porous Si was etched selectively and removed completely with the monocrystalline Si remaining unetched as an etch-stopping material. The etching rate of the nonporous monocrystalline Si was extremely low, the selection ratio of the etching rate of the porous Si being 10^5 or higher. Therefore, the decrease in thickness of the nonporous layer by etching was practically negligible (several tens of Å).

[0263] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm respectively on the two Si oxide films simultaneously. The monocrystalline Si layers did not change at all by the selective etching of the porous Si layer.

[0264] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0265] A plurality of semiconductor substrates having a semiconductor layer of high quality were prepared by repeating the above process in the same manner as in Example 1.

Example 6

[0266] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 5 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions below:

Current density:	7 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	4 minutes
Thickness of porous Si:	3 μm
Porosity:	15 %

[0267] The anodization was conducted further under the conditions below:

Current density:	30 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:3:2$
Time:	3 minutes
Thickness of porous Si:	10 μm
Porosity:	45 %

[0268] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 0.3 μm by CVD under the conditions below:

Source gas:	SiH_4
Carrier gas:	H_2
Temperature:	850°C
Pressure:	1 x 10^{-2} Torr
Growth rate:	3.3 nm/sec

[0269] The surface of the formed epitaxial Si layer was thermally oxidized to form SiO_2 layer in a thickness of 100 nm.

[0270] On the face of the SiO_2 layer, a separately prepared second Si substrate having a 500-nm thick SiO_2 layer was superposed with the SiO_2 layer inside, and the superposed matter was heat-treated at 700°C for 2 hours to bond the substrates tightly.

[0271] A sufficient pulling force was applied to the resulting bonded wafer in the direction perpendicular to the bonded wafer face in the same manner as in Example 1. Thereby, the porous Si layer was broken to allow the wafer to separate into two sheets with the porous Si layers exposed.

[0272] The porous Si on the second Si substrate was etched selectively with an etching solution of $HF/HNO_2/CH_3COOH$ type. Thereby the porous Si was etched selectively and removed completely. The etching rate of the nonporous monocrystalline Si was extremely low, so that the thickness decrease of the nonporous layer by etching was practicably negligible.

[0273] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm on the Si oxide film. The monocrystalline Si layers did not change at all by the selective etching of the porous Si layer.

[0274] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained. A plurality of semiconductor substrates having a semiconductor layer of high quality were prepared by repeating the above process in the same manner as in Example 1.

Example 7

[0275] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 6 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions below:

Current density:	5 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	12 minutes
Thickness of porous Si:	10 μm
Porosity:	15 %

[0276] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 1 gm by CVD under the growth conditions below:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 ℓ/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0277] The surface of the formed epitaxial Si layer was thermally oxidized to form SiO_2 layer in a thickness of 100 nm.

[0278] On the face of the SiO_2 layer, a separately prepared second Si substrate having a 500-nm thick SiO_2 layer was superposed with the SiO_2 layer inside, and the superposed matter was heat-treated at 900°C for 2 hours to bond the substrates tightly.

[0279] A sufficient pulling force was applied to the resulting bonded wafer in the direction perpendicular to the bonded wafer face in the same manner as in Example 1. Thereby, the porous Si layer was broken to allow the wafer to separate into two sheets with the porous Si layers exposed.

[0280] The porous Si layer on the second substrate was ground selectively by utilizing the monocrystalline layer as the stopper. Thereby the porous Si was removed selectively.

[0281] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm on the Si oxide film. The monocrystalline Si layers did not change at all by the selective grinding of the porous Si layer.

[0282] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0283] A plurality of semiconductor substrates having a semiconductor layer of high quality were prepared by repeating the above process in the same manner as in Example 1.

Example 8

[0284] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 6 inches, a thickness of 625 μm and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions below:

Current density:	5 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	12 minutes
Thickness of porous Si:	10 μm

Porosity:	15 %

[0285] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 1 μm by CVD under the conditions below:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 ℓ/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0286] The surface of the formed epitaxial Si layer was thermally oxidized to form SiO_2 layer in a thickness of 100 nm.

[0287] On the face of the SiO_2 layer, a separately prepared second Si substrate having a 500-nm thick SiO_2 layer was superposed with the SiO_2 layer inside, and the superposed matter was heat-treated at 900°C for 2 hours to bond the substrates tightly.

[0288] A supersonic energy was applied to the resulting bonded wafer in a vessel provided with a supersonic oscillator. Thereby, the porous Si layer was broken to allow the wafer to separate into two sheets with the porous Si layers exposed.

[0289] The porous Si layer on the second Si substrate was etched selectively with a mixture of 49% hydrofluoric acid with 30% hydrogen peroxide (1:5) with agitation. Thereby the porous Si was etched selectively and removed completely with the monocrystalline Si remaining unetched as an etch-stopping material. The etching rate of the nonporous monocrystalline Si was extremely low, the selection

ratio of the etching rate of the porous Si being 10^5 or higher. Therefore, the decrease in thickness of the nonporous layer by etching was practically negligible (several tens of Å).

[0290] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm on the Si oxide film. The monocrystalline Si layers did not change at all by the selective etching of the porous Si layer.

[0291] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0292] The first monocrystalline Si substrate was used repeatedly for the same use after removal of the porous Si remaining thereon.

Example 9

[0293] A first monocryatalline (100) Si substrate of P-type or N-type having a diameter of 4 inches, a thickness of 525 μm, and a specific resistance of 0.01 Ω.m was anodized in an HF solution under the anodization conditions as below:

Current density:	7 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	12 minutes
Thickness of porous Si:	10 μm
Porosity:	15 %

[0294] This substrate was oxidized at 400°C in an oxygen atmosphere for 2 hours. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si, monocrystalline Si was allowed to grow

epitaxially in a thickness of 0.5 μm by MBE (molecular beam epitaxy) under the growth conditions below:

Temperature:	700°C
Pressure:	1×10^{-9} Torr
Growth rate:	0.1 nm/sec
Temperature:	950°C
Growth rate:	0.3 μm/min

[0295] The surface of the epitaxially grown Si layer was thermally oxidized to form an SiO_2 layer of 100 nm thick.

[0296] On the face of the SiO_2 layer, was superposed a separately prepared fused quartz substrate, and the superposed matter was heat-treated at 400°C for 2 hours to bond the substrates.

[0297] The end of the porous layer was bared to the edge face of the wafer, and the porous Si is slightly etched. Thereto, a sharp blade like a shaver blade was inserted. Thereby, the porous layer was broken, and the wafer was separated into two sheets with the porous Si layers exposed.

[0298] The porous Si layer on the fused quartz substrate was etched selectively in a mixture of buffered hydrofluoric acid and 30% hydrogen peroxide (1:5) with agitation. Thereby the porous Si was etched and removed completely with the monocrystalline Si remaining unetched as an etch-stopping material. The etching rate of the nonporous monocrystalline Si was extremely low, the selection ratio of the etching rate of the porous Si being, 10^5 or higher. Therefore, the decrease in thickness of the nonporous layer by etching was practically negligible (several tens of Å).

[0299] Consequently, a monocrystalline Si layer was formed in a thickness of 0.5 μm on a fused quartz substrate. The monocrystalline Si layer did not change at all by the selective etching of the porous Si layer.

[0300] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0301] The same results were obtained without forming the oxide film of the surface of the epitaxial Si surface. The first monocrystalline Si substrate was used repeatedly for the same use after removal of the remaining porous Si and mirror-polishing of the surface.

Example 10

[0302] A first monocrystalline (100) Si substrate of P-type or N-type having a polished face on each side and having a diameter of 6 inches, a thickness of 625 μm and a specific resistance of 0.01 Ω.cm was anodized on both sides in an HF solution under the anodization conditions below:

Current density:	5 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	12 x 2 minutes
Thickness of porous Si:	10 μm each
Porosity:	15 %

[0303] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on both faces of the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 1 μm by CVD (chemical vapor deposition) under the conditions below:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 ℓ/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0304] The surfaces of the formed epitaxial Si layers were thermally oxidized to form SiO_2 layers in a thickness of 100 nm.

[0305] On each of the faces of the SiO_2 layers, a separately prepared second Si substrate having a 500-nm thick SiO_2 layer was superposed with the SiO_2 layer inside, and the superposed matter was heat-treated at 600°C for 2 hours to bond the substrates tightly.

[0306] The porous layers were bared at the edge face of the wafer, and a liquid such as water was allowed to penetrate into the porous Si. The entire bonded wafer was heated or cooled, whereby the porous Si layers were broken owing to expansion or other causes to allow the wafer to separate into three sheets with the porous Si layers exposed.

[0307] The porous Si layers were etched selectively with a mixture of 49% hydrofluoric acid with 30% hydrogen peroxide (1:5) with agitation. Thereby the porous Si was etched selectively and removed completely with the monocrystalline Si remaining unetched as an etch-stopping material. The etching rates of the nonporous monocrystalline Si was extremely low, the selection ratio of the etching rate of the porous Si being 10^5 or higher. Therefore, the decrease in thickness of the nonporous layer by etching was practically negligible (several tens of Å).

[0308] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm respectively on the two Si oxide films simultaneously. The monocrystalline Si layers did not change at all by the selective etching of the porous Si layer.

[0309] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0310] The same results were obtained without formation of the oxide film on the surface of the epitaxial Si layer.

[0311] The first monocrystalline Si substrate was used repeatedly for the same use after removal of the remaining porous Si and flattening of the surface by hydrogen treatment.

Example 11

[0312] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 5 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions below:

Current density:	7 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	4 minutes
Thickness of porous Si:	3 μm
Porosity:	15 %

[0313] The anodization was conducted further under the conditions below:

Current density:	30 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:3:2$
Time:	3 minutes

Thickness of porous Si:	10 μm
Porosity:	45 %

[0314] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 0.3 μm by CVD under the conditions below:

Source gas:	SiH_4
Carrier gas:	H_2
Temperature:	850°C
Pressure:	1 x 10^{-2} Torr
Growth rate:	3.3 nm/sec

[0315] The surface of the formed epitaxial Si layer was thermally oxidized to form a SiO_2 layer in a thickness of 100 nm.

[0316] The porous Si layer was etched selectively with an $HF/HNO_3/CH_3COOH$ type etching solution. Thereby the porous Si was etched selectively and removed completely. The etching rate of the nonporous monocrystalline Si was extremely low, so that the decrease in thickness of the nonporous layer by etching was practicably negligible.

[0317] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm on the Si oxide layer. The monocrystalline Si layer did not change at all by the selective etching of the porous Si layer.

[0318] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0319] The same results were obtained without forming the oxide film on the surface of the epitaxial Si layer surface.

[0320] The first monocrystalline Si substrate was used repeatedly for the same use after removal of the remaining porous Si.

Example 12

[0321] A first monocrystalline (100) Si substrate of P-type or N-type having a diameter of 5 inches, a thickness of 625 μm, and a specific resistance of 0.01 Ω.cm was anodized in an HF solution under the anodization conditions below:

Current density:	7 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	4 minutes
Thickness of porous Si:	3 μm
Porosity:	15 %

[0322] The anodization was conducted further under the conditions below:

Current density:	30 $mA.cm^{-2}$
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:3:2
Time:	3 minutes
Thickness of porous Si:	10 μm
Porosity:	45 %

[0323] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. Thereby the inner wall of the pores of the porous Si was covered with a thermal oxidation film. On the porous Si formed on the substrate, monocrystalline Si was allowed to grow epitaxially in a thickness of 0.3 μm by CVD under the conditions below:

Source gas:	SiH_4
Carrier gas:	H_2
Temperature:	850°C
Pressure:	1×10^{-2} Torr
Growth rate:	3.3 nm/sec

[0324] The surface of the formed epitaxial Si layer was thermally oxidized to form a SiO_2 layer in a thickness of 100 nm.

[0325] On the face of the SiO_2 layer, a separately prepared second Si substrate having a 500-nm thick SiO_2 layer was superposed with the SiO_2 layer inside, and the superposed matter was heat-treated at 700°C for 2 hours to bond the substrates tightly.

[0326] The porous layers were bared at the edge face of the wafer, and the porous Si was etched from the edge face with a selective etching solution, whereby the wafer came to be separated into two sheets.

[0327] Further, the porous Si layer on the second Si substrate was etched selectively with an $HF/HNO_3/CH_3COOH$ type etching solution. Thereby the porous Si was etched selectively and removed completely. The etching rate of the nonporous monocrystalline Si was extremely low, so that the thickness decrease of the nonporous layer by etching was practicably negligible.

[0328] Consequently, a monocrystalline Si layer was formed in a thickness of 1 μm on the Si oxide film. The monocrystalline Si layers did not change at all by the selective etching of the porous Si layer.

[0329] The cross-section of the Si layer was observed by transmission electron microscopy, and it was confirmed that no additional crystal defect was formed in the Si layer and the excellent crystallinity was retained.

[0330] The same results were obtained without forming the oxide film on the surface of the epitaxial Si layer surface.

[0331] The first monocrystalline Si substrate was used repeatedly for the same use after removal of the remaining porous Si.

[0332] A method is proposed in Japanese Patent Application No. 7-045441 for recycling the first substrate which is wasted in such a bonding method.

[0333] In this method, the following method is adopted, in the foregoing bonding and etch-back method using the porous Si, instead of the step for reducing in thickness the first substrate through grinding, etching or the like from the underside so as to expose the porous Si. This will be explained using Figs. 6A to 6E.

[0334] After forming a porous surface layer 172 of an Si substrate 171 (Fig. 6A), a single-crystal Si layer 173 is formed thereon (Fig. 6B). Then, the single-crystal Si layer 173 along with the Si substrate 171 is bonded to a main surface of another Si substrate 174, working as a support substrate, via an insulating layer therebetween (Fig. 6C). Thereafter, the bonded wafers are separated at the porous layer 172 and the porous Si layer 172 exposed on the surface at the side of the Si substrate 174 is selectively removed so that the SOI substrate is formed. Separation of the bonded wafers is performed, for example, a method selected from the following methods that the tensile force or pressure is sufficiently applied to the bonded wafers perpendicularly relative to an in-plane and uniformly over in-plane; that the wave energy such as the ultrasonic wave is applied; that the porous layer is exposed at the wafer end surfaces, the porous Si is etched to some extent, and what is like a

razor blade is inserted thereinto; that the porous layer is exposed at the wafer end surfaces and a liquid such as water is impregnated into the porous Si, and the whole bonded wafers are heated or cooled so as to expand the liquid. Alternatively, separation is performed by applying the force to the Si substrate 171 in parallel to the support substrate 174.

[0335] Each of these methods is based on the fact that, although the mechanical strength of the porous Si layer 172 differs depending on the porosity, it is considered to be much weaker than the bulk Si. For example, if the porosity is 50%, the mechanical strength can be considered to be half the bulk. Specifically, when a compressive, tensile or shear force is applied to the bonded wafers, the porous Si layer is first ruptured. As the porosity is increased, the porous layer can be ruptured with a weaker force.

[0336] However, if the porosity of porous silicon is increased, it is possible that distortion is introduced due to the ratio of bulk silicon relative to the lattice constant being increased so as to increase warpage of the wafer. As a result, the following problems may be raised, that is, the number of void bonding failure regions, called voids is increased upon bonding, the crystal defect density is increased and, in the worst case, cracks are introduced into the epitaxial layer, and slip lines are introduced on the periphery of the wafer due to the influence of thermal distortion upon the epitaxial growth.

[0337] When applying the force in the vertical or horizontal direction relative to the surface of the wafer, since the semiconductor substrate is not a fully rigid body but an elastic body, the wafer may be subjected to elastic deformation depending on a supporting fashion of the wafer so that the force escapes and thus is not applied to the porous layer effectively. Similarly, when inserting what is like a razor blade from the wafer end surface, unless the razor blade is fully thin and fully high in rigidity, the yield may be lowered.

[0338] Further, if the bonding strength at the bonded interface is weaker as compared with the strength of the porous Si layer or if weak portions exist locally, the two wafers may be separated at the bonded interface so that the initial object cannot be achieved.

[0339] Further, since, in any of the methods, the position where separation occurs in the porous layer is not fixed, if the ratio in etching speed between the porous Si and the bulk Si is not sufficient, the epitaxial silicon layer is first etched more or less at a portion where the porous layer remains thin rather than at a portion where the porous layer remains thick. Thus, the thickness uniformity of the SOI layer may deteriorate. Particularly, when the final thickness of the SOI layer is reduced to about 100nm, the thickness uniformity is deteriorated so that a problem may result when forming the element, such as the fully depleted MOSFET, whose threshold voltage is sensitive to the film thickness.

[0340] Japanese Patent Application No. 5-211128 (corresponding to United States Patent No. 5,374,564) discloses a method for producing the SOI. In this method, hydrogen ions are directly implanted into a single-crystal Si substrate, and then the single-crystal Si substrate and a support substrate are bonded together. Finally, the single-crystal Si substrate is separated at a layer where hydrogen ions are implanted, so as to form the SOI. In this method, since hydrogen ions are directly implanted into the single-crystal Si substrate which is then separated at the ion-implanted layer, the flatness of the SOI layer is not good. Further, the thickness of the SOI layer is determined by the projection range, so that the degree of freedom of the thickness is low. Further, it is necessary to select an implanting condition satisfying both the layer thickness and the separation, which creates a difficulty in control. Further, in case of aiming at obtaining a thin layer, the thickness of which cannot be determined by the ion implantation, it is necessary to carry out a reducing process in thickness such as grinding and etching, which

process is nonselective, so that there is a fear of deteriorating uniformity of the thickness.

[0341] In view of the foregoing, a method has been demanded for producing, with high reproducibility, a high quality SOI substrate and whose SOI layer is extremely flat, while simultaneously saving resources and reducing costs through recycling of the wafer.

[0342] On the other hand, in general, on a light transmittable substrate, typically glass, the deposited thin Si layer only becomes amorphous or polycrystalline at best, reflecting disorderliness in crystal structure of the substrate, so that a high-performance device cannot be produced. This is due to the crystal structure of the substrate being amorphous, and thus an excellent single-crystal layer cannot be achieved by merely depositing the Si layer.

[0343] The light transmittable substrate is important for constituting a contact sensor as being a light-receiving element or a projection-type liquid-crystal image display device. To achieve further densification, higher resolution and increased fineness of picture elements of the sensor or the display device, a high-performance drive element is required. As a result, it is necessary to produce the element on the light transmittable substrate using the single-crystal layer having an excellent crystalline property.

[0344] Further, when using the single-crystal layer, reduction in size and acceleration of a chip can be achieved by incorporating a peripheral circuit for driving the picture elements and an image processing circuit into the same substrate having the picture elements.

[0345] Specifically, in case of amorphous Si or polycrystalline Si, it is difficult, due to its defective crystal structure, to produce the drive element having the performance which is required or will be required in the future.

[0346] On the other hand, to produce the compound semiconductor device, the substrate of the compound semiconductor is essential. However, the compound semiconductor substrate is expensive and further is very difficult to increase in area.

[0347] An attempt has been made to achieve the epitaxial growth of the compound semiconductor such as GaAs on the Si substrate. However, due to differences in lattice constant or thermal expansion coefficient, the grown film is poor in crystalline property and thus is very difficult to apply to the device.

[0348] Further, an attempt has been made to achieve the epitaxial growth of the compound semiconductor on porous Si to reduce misfit of the lattice. However, due to low thermostability and age deterioration of porous Si, its stability and reliability are poor as the substrate during or after production of the device. However, there is a problem that the compound semiconductor substrate is expensive and low in mechanical strength so that the large-area wafer is difficult to produce.

[0349] In view of the foregoing, an attempt has been made to achieve the heteroepitaxial growth of a compound semiconductor on a Si wafer which is inexpensive and high in mechanical strength so that a large-area wafer can be produced.

[0350] Recently, attention has been given to porous silicon as a luminescent material for photoluminescence, electroluminescence or the like, and many research reports have been made. In general, the structure of porous silicon largely

differs depending on the type (p, n) and the concentration of impurities contained in the silicon. When the p-type impurities are doped, the structure of porous silicon is roughly divided into two kinds depending on whether the impurity concentration is no less than $10^{18}/cm^3$ or no more than $10^{17}/cm^3$. In the former case, the pore walls are relatively thick, that is, from several nanometers to several tens of nanometers, the pore density is about $10^{11}/cm^2$ and the porosity is relatively low. However, it is difficult for this porous silicon to luminesce. On the other hand, in the latter case, as compared with the former case, porous silicon whose pore wall is no more than several nanometers in thickness, whose pore density is greater by one figure order of magnitude and whose porosity exceeds 50%, can be easily formed. Most luminous phenomena, such as photoluminescence, are mainly based on the formation of porous silicon using the latter as a starting material. However, the mechanical strength is low due to the large porosity. Further, since a lattice constant deviation relative to bulk Si is as much as 10^{-3} (about 10^{-4} in the former case), there has been a problem that, when epitaxial-growing the single-crystal silicon layer on such porous silicon, defects are largely introduced into the epitaxial Si layer and cracks are further introduced thereinto. On the other hand, for utilizing the fine porous structure, which is suitable for a luminescent material, as a luminescent element, it has been desired that the epitaxial Si layer be formed on porous silicon for providing a contact or the MOSFET or the like as a peripheral circuit to be formed on the epitaxial silicon layer.

[0351] The present invention simultaneously solves the foregoing various problems by superposing a finer porous structure in the foregoing porous layer.

[0352] It has been reported that, by performing ion implantation of helium or hydrogen into bulk silicon and applying heat thereto, micro-cavities having diameters in the range from several nanometers to several tons of nanometers are formed at the implanted region in the density of as much as 10^{16} to $10^{17}/cm^3$ (for example, A. Van Veen, C.C. Griffioen, and J.H. Evans, Mat. Res. Soc. Symp.

Proc. 107 (1988, Material Res. Soc. Pittsburgh, Pennsylvania) p. 449). Recently, utilizing these micro-cavity groups as gettering sites of metal impurities has been investigated.

[0353] V. Raineri and S.U. Campisano implanted helium ions into bulk silicon and applied a heat treatment thereto to form the cavity groups, then exposed the sides of the cavity groups by forming grooves in the substrate and applied an oxidation treatment thereto. As a result, the cavity groups were selectively oxidized to form a buried silicon oxide layer. That is, they reported that the SOI structure could be formed (V. Raineri and S.U. Campisano, Appl. Phys. Lett. 66 (1995) p. 3654). However, in their method, thicknesses of the surface silicon layer and the buried silicon oxide layer were limited to achieve both formation of the cavity groups and relaxation of stresses introduced due to volume expansion upon oxidation and further the formation of the grooves were necessary for selective oxidation so that the SOI structure could not be formed all over the substrate. Such formation of the cavity groups has been reported as a phenomenon following the implantation of light elements into metal along with an expansion or separation phenomenon of the cavity groups as a part of the research about a first reactor wall of the nuclear fusion reactor.

[0354] Porous Si was found in the course of the research of electropolishing of the semiconductor in 1956 by Uhlir and collaborator (A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956)). Porous silicon can be formed by anodizing the Si substrate in the HF solution. Unagami and collaborator researched the dissolution reaction of Si in the anodization and reported that positive holes were necessary for the anodizing reaction of Si in the HF solution and the reaction was as follows (T. Unagami, J. Electrochem. Soc., vol. 127, 476 (1980)):

$$Si + 2HF + (2-n)\,e^{+} \rightarrow SiF_2 + 2H^{+} + ne^{-}$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (4-\lambda)\, e^+ \rightarrow SiF_4 + 4H^+ + \lambda e^-$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

wherein e^+ and e^- represent a hole and an electron, respectively, and n and λ represent the numbers of holes necessary for dissolution of one Si element, respectively. It was reported that porous Si was formed when $n>2$ or $\lambda>4$ was satisfied.

[0355] As appreciated from the foregoing, p-type Si having the holes is rendered porous while n-type Si is not rendered porous. The selectivity while getting porous has been proved by Nagano and collaborators and Imai (Nagano, Nakajima, Yasuno, Oonaka, Kajiwara, Engineering Research Report of Institute of Electronics and Communication Engineers of Japan, vol. 79, SSD799549 (1979)), (K. Imai, Solid-State Electronics, vol. 24, 159 (1981)).

[0356] However, there have also been reports that high-concentration n-type Si can be rendered porous (R.P. Holmstrom and J.Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983)) so that it is important to choose the substrate which can be rendered porous, irrespective of p- or n-type.

[0357] Porous silicon can be formed by anodizing the Si substrate in the HF solution. The porous layer has a structure like sponge including holes of about 10^{-1} to 10nm in diameter arranged at intervals of about 10^{-1} to 10nm. The density thereof can be changed in the range of 1.1 to 0.6g/cm^3 by changing the HF solution concentration in the range of 50 to 20% and by changing the current density, as compared with the density 2.33g/cm^3 of the single-crystal Si. That is, the porosity can be changed. Although the density of porous Si is no more than half as compared with the single-crystal Si as described above, the monocrystalline property is maintained so that the single-crystal Si layer can be epitaxially grown at the upper part of the porous layer. However, at a temperature not less than

1,000°C, rearrangement of the internal holes occurs to spoil the accelerating etching characteristic. In view of this, it has been said that the low temperature growth, such as molecular beam epitaxial growth, plasma CVD, vacuum CVD, optical CVD, bias sputtering or liquid deposition, is suitable for the epitaxial growth of the Si layer. On the other hand, if a protective film is formed in advance on the pore walls of the porous layer by means of the method of low temperature oxidation or the like, high temperature growth is also possible.

[0358] Further, the porous layer is reduced in density to no more than half due to the formation of a lot of the internal cavities therein. As a result, since the surface area is greatly increased as compared with the volume, the chemical etching speed thereof is extremely increased as compared with the etching speed of the normal single-crystal layer.

[0359] Although the mechanical strength of porous Si differs depending on porosity, it is considered to be smaller than that of bulk Si. For example, if porosity is 50%, the mechanical strength can be considered to be half the bulk. Specifically, when a compressive, tensile or shear force is applied to the bonded wafers, the porous Si layer is ruptured first. As the porosity is increased, the porous layer can be ruptured with a weaker force.

[0360] The present invention simultaneously solves the foregoing various problems by superposing a finer porous structure in the foregoing porous layer.

[0361] It has been found that, when ion implantation of at least one kind of noble gas, hydrogen and nitrogen is performed into the porous layer with a projection range ensured, the porosity of the implanted region is increased. When observing in detail the implanted layer using an electron microscope, a lot of micro-cavities were formed in the pore walls of the porous layer formed in advance. Specifically,

the fine porous structure was formed. Upon irradiation of ultraviolet light, the luminous phenomenon at the wavelength around 700nm was confirmed.

[0362] If choosing further implantation conditions, porous silicon can be separated at a depth corresponding to the projection range of the ion implantation.

[0363] The separation can be improved in uniformity or achieved with less implantation amount by forming in advance a thin film on the pore walls of porous silicon using the method of particularly low temperature oxidation. The separation can be facilitated by applying the heat treatment after the ion implantation.

[0364] By ion-implanting at least one kind of noble gas, hydrogen and nitrogen into the porous layer with a projection range ensured after formation of at least one layer of non-porous film, such as a non-porous single-crystal silicon layer, on porous silicon or without such formation, the porosity of the implanted layer is increased. If such a Si substrate is bonded to the support substrate and then the bonded substrates are subjected to the mechanical force or the heat treatment, or even without such processes, the two bonded substrates can be separated into two at a portion of the porous silicon layer where ions are implanted.

[0365] By supporting both sides of the ion-implanted layer with a fully thick elastic or rigid body, the separation can be achieved uniformly over a large area. Further, it is possible to facilitate the separation of the substrates by applying heat treatment, force or ultrasonic waves to the substrates.

[0366] Even if non-formation regions of the implanted layer are formed due to presence of the foreign matter on the surface upon the ion implantation, since the mechanical strength of the porous layer itself is smaller than bulk Si, separation occurs in the porous layer. Thus, the two bonded substrates can be separated without causing cracks or lines in the non-porous single-crystal Si layer. In other

words, the phenomenon of the separation can be selected by selecting timing for the manifestation from the time of implantation and the time of heat treatment; and a condition of implantation such as an amount of implanted beam and energy thereof. Further, the layer having a large porosity may be formed at a region of a constant depth from the surface of the porous layer by controlling the condition at anodization.

[0367] Further, by selectively removing the porous Si layer remaining on the surface of the separated substrate using the method of etching, polishing or the like, the single-crystal Si layer is exposed on the support substrate. on the other hand, after removing the remaining porous Si, the Si substrate can be again formed with porous silicon, then formed with a single-crystal Si layer and subjected to the ion implantation of at least one kind of noble gas, hydrogen and nitrogen into the porous layer with the projection range ensured, and then bonded to a support substrate. That is, the Si substrate can be recycled. Further, if the Si substrate, with the porous silicon layer remaining, is subjected to heat treatment in the reducing atmosphere including hydrogen or the like, the porous silicon surface is rendered flat and smooth so that the single-crystal silicon layer can be formed successively. By bonding the single-crystal silicon layer to the support substrate, the Si substrate can also be recycled.

[0368] According to this method, since the portion to be separated is limited to the ion-implanted region in the porous layer, the depth of the separated region is not dispersed in the porous layer. Thus, even if the ratio for selectively etching porous silicon is insufficient, porous silicon can be removed for substantially a constant time so that the uniformity of the thickness of the single-crystal silicon layer provided on the support substrate is not spoiled.

[0369] In the conventional method of producing the bonded substrates, the Si substrate is gradually removed from one side thereof through grinding or etching.

Thus, it is impossible to effectively use both sides of the Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the Si substrate is held in the initial state other than its surface layers so that, by using both sides of the Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one Si substrate. As appreciated, also in this case, the Si substrate can be recycled as an Si substrate after removing the remaining porous Si.

[0370] The support substrate may be, for example, a light transmittable substrate, such as a Si substrate, a Si substrate with a silicon oxide film formed thereon, a silica glass substrate or a glass substrate, or a metal substrate, but not particularly limited thereto.

[0371] The thin film formed on the porous Si layer on the Si substrate may be, for example, a non-porous single-crystal Si film, a compound semiconductor film such as GaAs or InP, a metal film or a carbon film, but not particularly limited thereto. Further, the thin film is not necessarily formed all over the porous Si layer, but may be partially etched by the patterning process.

[Embodiment 6]

[0372] As shown in Fig. 7A, a Si single-crystal substrate 111 is first prepared and then rendered porous at its surface layer. Numeral 112 denotes the resulting porous layer. As shown in Fig. 7B, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 112. Then, a porous layer 113 having large porosity is formed in the porous layer 112. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the

micro-cavities to be formed are changed, but approximately no less than $1x10^{13}/cm^2$ and more preferably $1x10^{14}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, heat treatment is performed if necessary. In the case of the heat treatment atmosphere being an oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overoxidation.

[0373] When the light of a mercury lamp, a xenon lamp or the like is applied to the thus produced sample as the light of shorter wavelength, the sample emits the red light around 780nm. That is, the photoluminescence is confirmed. Or an EL (Electroluminescence) element can be formed.

[0374] In Fig. 7B, the semiconductor substrate of the present invention is shown. The layer 113 is the porous Si layer with the large porosity obtained as the result of the foregoing ion implantation. The fine porous structure showing the luminous phenomenon is formed uniformly in a large area all over the wafer. Further, the metallic luster is held on the surface, that is, not showing the stained manner as in the prior art, so that metallic wiring can be easily arranged.

EMBODIMENT 7

[0375] As shown in Fig. 8A, a Si single-crystal substrate 121 is first prepared and then rendered porous at its surface layer. Numeral 122 denotes the resulting porous layer. As shown in Fig. 8B, at least one kind of noble gas, hydrogen and nitrogen is ion-planted into the porous layer 122. Then, a porous layer (ion-implanted layer) 123 having large porosity is formed in the porous layer 122. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the

density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed or at least one of compressive, tensile and shear stresses is applied to the wafer in a direction perpendicular to the surface as necessary, so as to divide the semiconductor substrate into two at the ion-implanted layer as a border. In the case of the heat treatment atmosphere being an oxidizing atmosphere, the pore walls are oxidized so that attention should be given to preventing the Si region from being all changed into silicon oxide due to over-oxidation.

[0376] In Fig. 8C, the extremely thin porous substrate obtained by the present invention is shown. Since the division of the substrate starts spontaneously upon the heat treatment or the like as a trigger due to the internal stress introduced upon the implantation, the extremely thin porous structure can be formed uniformly all over the substrate. The pores of the porous structure are formed from one main surface of the substrate toward the other main surface. Accordingly, when the gas is implanted under pressure from the one main surface, it is ejected out from the other main surface. In this case, since the pore size of the porous structure is in the range from several nanometers to several tens of nanometers, a particle greater than this cannot pass therethrough. On the other hand, although pressure loss is caused depending on the pore size, the pore density and a thickness of the extremely thin porous substrate, the strength of the substrate and the pressure loss can be both within the practical range if the thickness of the porous layer is approximately no more than 20μm.

EMBODIMENT 8

[0377] As shown in Fig. 9A, a Si single-crystal substrate 131 is first prepared and then rendered porous at its surface layer. Numeral 132 denotes the resulting

porous layer. Subsequently, as shown in Fig. 9B, at least one layer 133 is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like.

[0378] As shown in Fig. 9C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 132. Then, a porous layer 134 having large porosity is formed in the porous layer 132. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, heat treatment is performed as necessary. In the case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to preventing the Si region from being all changed into silicon oxide due to overoxidation.

[0379] When the light of a mercury lamp, a xenon lamp or the like is applied to the thus produced sample as the light of shorter wavelength, the sample emits the red light around 780nm. That is, the photoluminescence is confirmed. Or an EL element can be formed.

[0380] The EL element shown in Figs. 10A-10B is realized by forming a construction where a voltage is applied to a porous layer having a large porosity formed in the porous layer by means of ion implantation and so forth. For example, when turning p^+ substrate 121 porous, the EL element is realized by implanting phospho-ion and so forth in porous layer 122 including porous layer 123 having a large porosity from the surface in a manner of making the ion reach a

region of a constant depth from the surface, or by diffusing the ion by means of heat diffusion etc., to form a p-n junction in porous layer 123 having a large porosity or in the neighborhood thereof. A portion 127 is an n-region of the porous layer having a large porosity, which region is obtained as a result of the above-mentioned process.

[0381] Electrodes 125 and 126 are secured with the substrate and the surface of the porous portion. The electrodes may be formed in the side of the surface of the porous portion by a process comprised of forming epitaxial Si layer 124 on the porous portion prior to the formation of the electrode and then forming the electrode thereon (see Fig. 10C). Further, as shown in Fig. 10D, the epitaxial Si layer may be removed partly as the occasion demands so as to facilitate the penetration of the light of the EL.

[0382] In Fig. 3B, the semiconductor substrate of the present invention is shown. The fine porous structure showing the luminous phenomenon is formed uniformly in a large area all over the wafer. Further, the metallic luster is held on the surface, that is, not showing the cracks or the like as in the prior art, so that metallic wiring can be easily arranged.

EMBODIMENT 9

[0383] As shown in Fig. 11A, a Si single-crystal substrate 141 is first prepared and then rendered porous at its surface layer. Numeral 142 denotes the resulting porous layer. Subsequently, as shown in Fig. 11B, at least one non-porous thin film 143 is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like. Or an element structure such as a MOSFET may be formed.

[0384] As shown in Fig. 11C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 142 so as to form an implanted layer 144. When observing the implanted layer by a transmission electron microscope, formation of numberless micro-cavities can be seen. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed as necessary. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to preventing the Si region from being all changed into silicon oxide due to overoxidation.

[0385] As shown in Fig. 11D, after abutting a support substrate 145 and the surface of the first substrate with each other at room temperature, they are bonded to each other through anodic bonding, pressurization, heat treatment or a combination thereof. As a result, both substrates are firmly coupled with each other.

[0386] When single-crystal Si is deposited, it is preferable to perform the bonding after oxidized Si is formed on the surface of single-crystal Si through thermal oxidation or the like. On the other hand, the support substrate can be selected from among a Si substrate, a Si substrate with a silicon oxide film formed thereon, a light transmittable substrate such as quartz, a sapphire substrate and the like, but not limited thereto as long as the surface serving for the bonding is fully flat. The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

[0387] Subsequently, the substrates are divided at the ion-implanted layer 144 in the porous Si layer 142 (Fig. 11E). The structure of the second substrate side includes the porous Si layer 142, the non-porous thin film (for example, the single-crystal Si layer) 143 and the second substrate 145.

[0388] Further, the porous Si layer 142 is selectively removed. In case of the non-porous thin film being single-crystal Si, only the porous Si layer 142 is subjected to the electroless wet chemical etching using at least one of the normal Si etching liquid, hydrofluoric acid being the porous Si selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to buffered hydrofluoric acid, so as to render the film formed in advance on the porous layer of the first substrate remaining on the second substrate. As described above in detail, only the porous Si layer can be selectively etched using the normal Si etching liquid due to the extensive surface area of porous Si. Alternatively, the porous Si layer 142 may be removed through selective polishing using the single-crystal Si layer as a polishing stopper.

[0389] In the case where the compound semiconductor layer is formed on the porous layer, only the porous Si layer 142 is subjected to chemical etching using the etching liquid which has the greater etching speed for Si relative to the compound semiconductor, so that the thickness-reduced single-crystal compound semiconductor layer 143 remains on the insulating substrate 145. Alternatively, the porous Si layer 142 is removed through selective polishing using the single-crystal compound semiconductor layer 143 as a polishing stopper.

[0390] In Fig. 11F, the semiconductor substrate of the present invention is shown. On the insulating substrate 145, the non-porous thin film, such as the single-crystal

Si thin film 143, is formed in a large area all over the wafer, flatly and uniformly reduced in thickness. The semiconductor substrate thus obtained can be suitably used in production of an insulated electronic element.

[0391] The Si single-crystal substrate 141 can be reused as a Si single-crystal substrate 141 after removing any remaining porous Si and after performing surface-flattening if the surface flatness makes the substrate unusable.

[0392] Alternatively, a non-porous thin film may be again formed without removing porous Si so as to provide the substrate as shown in Fig. 11B, which is then subjected to the processes shown in Figs. 11C to 11F.

EMBODIMENT 10

[0393] As shown in Fig. 12A, a Si single-crystal substrate 151 is first prepared and then rendered porous at both surface layers thereof. Numerals 152 and 153 denote the obtained porous layers. Subsequently, as shown in Fig. 12B, at least one non-porous thin film 154, 155 is formed on each of the porous layers. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like. Or an element structure such as a MOSFET may be formed.

[0394] As shown in Fig. 12C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layers 152 and 153 so as to form implanted layers 156 and 157. When observing the implanted layers by a transmission electron microscope, formation of numberless micro-cavities can be seen, and accordingly the porosity enlarges. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired.

Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but they are approximately no less than $10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range deeper, channeling ion implantation may be employed. After the implantation, heat treatment is performed as necessary. In the case of the heat treatment atmosphere being an oxidizing atmosphere, the pore walls are oxidized so that attention should be given to preventing the Si region from being all changed into silicon oxide due over oxidation.

[0395] As shown in Fig. 12D, after abutting two support substrates 158 and 159 and the surfaces of the non-porous thin films 154 and 155 of the first substrate with each other at room temperature, they are bonded to each other through anode bonding, pressurization, heat treatment or a combination thereof. As a result, the three substrates are firmly coupled with each other.

[0396] Alternatively, the bonding may be performed in five plies with insulating thin plates interposed therebetween.

[0397] When single-crystal Si is deposited, it is preferable to perform the bonding after oxidized Si is formed on the surface of single-crystal Si through thermal oxidation or the like. On the other hand, the support substrate can be selected from among a Si substrate, a Si substrate with a silicon oxide film formed thereon, a light transmittable substrate such as quartz, a sapphire substrate and the like, but not limited thereto as long as the surface serving for the bonding is completely flat.

[0398] The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

[0399] Subsequently, the substrates are divided at the ion-implanted layers 156 and 157 in the porous Si layers 152 and 153 (Fig. 12E). The structure of each of

the two support substrate sides includes the porous Si layer 152, 153, the non-porous thin film (for example, the single-crystal Si layer) 154, 155 and the support substrate 158, 159.

[0400] Further, the porous Si layer 152, 153 is selectively removed. In case of the non-porous thin film being single-crystal Si, only the porous Si layer 152, 153 is subjected to the electroless wet chemical etching using at least one of the normal Si etching liquid, hydrofluoric acid being the porous Si selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to buffered hydrofluoric acid, so that the film formed in advance on the porous layer of the first substrate remains on the support substrate. As described above in detail, only the porous Si layer can be selectively etched using the normal Si etching liquid due to the extensive surface area of porous Si.

[0401] Alternatively, the porous Si layer 152, 153 may be removed through selective polishing using the single-crystal Si layer 154, 155 as a polishing stopper.

[0402] In the case where the compound semiconductor layer is formed on the porous layer, only the porous Si layer 152, 153 is subjected to chemical etching using the etching liquid which has the greater etching speed for Si relative to the compound semiconductor, so that the thickness-reduced single-crystal compound semiconductor layer 154, 155 remains on the insulating substrate. Alternatively, the porous Si layer 152, 153 is removed through selective polishing using the single-crystal compound semiconductor layer 154, 155 as a polishing stopper.

[0403] In Fig. 12F, the semiconductor substrates of the present invention are shown. On the support substrates, the non-porous thin films, such as the single-crystal Si thin films 154 and 155, are formed in large area all over the wafer, flatly

and uniformly reduced in thickness, so that the two semiconductor substrates are simultaneously formed. The semiconductor substrates thus obtained can be suitably used also in view of production of the insulated electronic elements.

[0404] The first Si single-crystal substrate 151 can be reused as a first Si single-crystal substrate 151 after removing remaining porous Si and after performing surface flattening if the surface flatness makes it unusable. Alternatively, a non-porous thin film may be again formed without removing porous Si so as to provide the substrate as shown in Fig. 12B, which is then subjected to the processes shown in Figs. 12C to 12F. The support substrates 158 and 159 are not necessarily identical with each other.

EMBODIMENT 11

[0405] The eleventh preferred embodiment will be described with reference to Figs. 13A to 13E.

[0406] First, a single-crystal Si substrate 100 is anodized to form a porous Si layer 101 (Fig. 13A). In this case, a thickness to be rendered porous is in the range from several micrometers to several tens of micrometers on one surface layer of the substrate. It may be arranged to anodize the whole Si substrate 100.

[0407] The method of forming porous silicon will be explained using Figs. 14A and 14B. First, as the substrate, a p-type single-crystal silicon substrate 600 is prepared. An n-type may also be used. However, in this case, it is necessary that the substrate is limited to a low-resistance substrate or that the light is applied onto the surface of the substrate so as to facilitate generation of the holes. The substrate 600 is set in an apparatus as shown in Fig. 14A. Specifically, one side of the substrate is in contact with hydrofluoric acid solution 604 having therein a negative electrode 606, while the other side of the substrate is in contact with a positive

metal electrode 605. On the other hand, as shown in Fig. 14B, a positive electrode 605' may also be provided in a solution 604'. In any case, the substrate is first rendered porous from the negative electrode side abutting the hydrofluoric acid solution. As the hydrofluoric acid solution 604, concentrated hydrofluoric acid (49%HF) is used in general. As diluted by pure water (H_2O), although depending on current values, etching occurs from a certain concentration so that it is not preferable. During anodization, bubbles are generated from the surface of the substrate 600. Alcohol may be added as a surface active agent for effective removal of the bubbles. As alcohol, methanol, ethanol, propanol, isopropanol or the like is used. Instead of the surface active agent, an agitator may be used to agitate the solution so as to achieve anodization. The negative electrode 606 is made of a material, such as gold (Au) or platinum (Pt), which does not corrode relative to the hydrofluoric acid solution. A material of the positive electrode 605 may be metal which is used in general. On the other hand, since the hydrofluoric acid solution 604 reaches the positive electrode 605 when anodization is achieved relative to the whole substrate 600, it is preferable to coat the surface of the positive electrode 605 with a metal film which is resistive to the hydrofluoric acid solution. The maximum current value for anodization is several hundreds of mA/cm^2, while the minimum current value therefor is arbitrary, other than zero. This current value is determined in range where the good-quality epitaxial growth is achieved on the surface of porous silicon. In general, as the current value increases, the anodization speed increases and the density of the porous Si layer decreases. That is, the volume of the pores increases. This changes the condition of the epitaxial growth.

[0408] On the porous layer 101 thus formed, a non-porous single-crystal silicon layer 102 is epitaxially grown (Fig. 13B).

[0409] Subsequently, the surface of the epitaxial layer 102 is oxidized (including thermal oxidation) so as to form an SiO_2 layer 103 (Fig. 13C). This is necessary

because, if the epitaxial layer is directly bonded to the support substrate in the next process, impurities tend to segregate at the bonded interface and dangling bonds of atoms at the interface increase, which will cause the thin film device to be unstable. However, this process is not essential, but may be omitted in a device structure wherein such phenomena are not serious. The SiO_2 layer 103 works as an insulating layer of the SOI substrate and should be formed on at least one side of the substrate to be bonded. There are various ways to form the insulating layer.

[0410] Upon oxidation, a thickness of the oxidized film is set to a value which is free of contamination taken into the bonded interface from the atmosphere.

[0411] Thereafter, the foregoing ion implantation is performed to form a layer with large porosity in the porous Si layer 101.

[0412] The substrate 100 having the foregoing epitaxial surface with the oxidized surface and a support substrate 110 having an SiO_2 layer 104 on the surface are prepared. The support substrate 110 may be a silicon substrate whose surface is oxidized (including thermal oxidation), quartz glass, crystallized glass, an arbitrary substrate with SiO_2 deposited thereon, or the like. A silicon substrate without the SiO_2 layer 104 may also be used as the support substrate.

[0413] The foregoing two substrates are bonded together after cleaning them (Fig. 13D). The cleaning is performed pursuant to the process of cleaning (for example, before oxidation) the normal semiconductor substrate. By pressurizing the whole substrate after the bonding, the bonding strength can be enhanced.

[0414] Subsequently, the bonded substrates are subjected to heat treatment. Although the higher temperature is preferable for the heat treatment, if it is too high, the porous layer 101 tends to cause structural change or the impurities contained in the substrate tend to be diffused into the epitaxial layer. Thus, it is

necessary to select temperature and time which does not cause these problems. Specifically, about 600 to 1,100°C is preferable. On the other hand, there are substrates that cannot be subjected to thermal treatment at the high temperature. For example, in case of the support substrate 110 being made of quartz glass, it can be subjected to the thermal treatment only at the temperature no greater than 200°C due to differences in the thermal expansion coefficients between silicon and quartz. If this temperature is exceeded, the bonded substrates may be separated or ruptured due to stress. The thermal treatment is sufficient as long as it can endure the stress upon grinding or etching of the bulk silicon 100 performed in the next process. Accordingly, even at the temperature no greater than 200°C, the process can be performed by optimizing the surface processing condition for activation.

[0415] Then, by the foregoing method, the substrates are separated into two at the porous Si layer having the large porosity. The layer having the large porosity can be formed by altering current in the anodization, besides the ion implantation.

[0416] Subsequently, the silicon substrate portion 100 and the porous portion 101 are selectively removed with the epitaxial layer 102 remaining (Fig. 13E). In this fashion, the SOI substrate is obtained.

[0417] The following processes may be added to the foregoing processes:

(1) The thickness of the wall between the adjacent holes in the oxidized (preoxidation) porous silicon layer, of i.e. the pore internal walls of the porous layer is very small, that is, several nanometers to several tens of nanometers. Thus, if the high-temperature process is applied to the porous layer upon formation of the epitaxial silicon layer or upon heat treatment after bonding, the pore wall may agglomerate and enlarge so that the pore wall may clog the pore and lower the etching speed. In view of this, after formation of the porous layer, a thin oxidized film is formed on the pore wall so as to suppress the enlargement of the pore wall.

On the other hand, since it is necessary to epitaxially grow the non-porous single-crystal silicon layer on the porous layer, it is necessary to oxidize only the surface of the pore inner wall such that the monocrystalline property remains inside the pore wall of the porous layer. It is preferable that the oxidized film is in the range of several angstroms to several tens of angstroms. The oxidized film of such a thickness is formed through heat treatment in an oxygen atmosphere at the temperature of 200°C to 700°C, and more preferably 250°C to 500°C.

(2) Hydrogen Baking Process

[0418] The present inventors have shown in the Publication No. EP553852A2 that, through heat treatment in a hydrogen atmosphere, small roughness on the silicon surface can be removed to obtain very smooth silicon surface. Also in the present invention, baking in the hydrogen atmosphere can be applied. The hydrogen baking can be performed, for example, after formation of the porous silicon layer and before formation of the epitaxial silicon layer. Apart from this, the hydrogen baking can be performed to the SOT substrate obtained after etching removal of the porous silicon layer. Through the hydrogen baking process performed before formation of the epitaxial silicon layer, a phenomenon occurs that the pore surface is closed due to migration of silicon atoms forming the porous silicon surface. When the epitaxial silicon layer is formed in the state where the pore surface is closed, the epitaxial silicon layer with fewer crystal defects can be achieved. On the other hand, through the hydrogen baking process performed after etching of the porous silicon layer, the epitaxial silicon surface which was more or less roughened by etching can be smoothed out, and boron from the clean room inevitably taken into the bonded interface upon bonding and boron thermally diffused in the epitaxial Si layer from the porous Si layer can be removed.

EMBODIMENT 12

[0419] The twelfth preferred embodiment will be described with reference to Figs. 15A to 15G. Numerals in Figs. 15A to 15G which are the same as those in Figs. 13A to 13E represent the same portions in Figs. 13A to 13E. In the embodiment shown in Figs. 13A to 13E, the surfaces of the two substrates to be bonded are the SiO_2 layer 103 and the SiO_2 layer 104. However, both of these surfaces are not necessarily the SiO_2 layers, but at least one of them may be made of SiO_2. In this preferred embodiment, the surface of an epitaxial silicon layer 1102 formed on a porous silicon layer is bonded to the surface of an oxidized film 1104 formed on a silicon substrate 1110, and the surface of an oxidized film 1103 formed by thermal oxidation of the surface of the epitaxial silicon layer 1102 is bonded to the surface of the silicon substrate 1110 which is not oxidized. In this preferred embodiment, the other processes can be performed as in the embodiment shown in Figs.13A to 13E.

EMBODIMENT 13

[0420] The thirteenth preferred embodiment will be described with reference to Figs. 16A to 16G. Numerals in Figs. 16A to 16G which are the same as those in Figs. 13A to 13E represent the same portions in Figs. 13A to 13E. In this preferred embodiment, a substrate bonded to a substrate formed with an epitaxial silicon film is made of a glass material 1210, such as quartz glass or blue glass. In this preferred embodiment, an epitaxial silicon layer 1102 is bonded to the glass substrate 1210, and an oxidized film 1103 formed by thermal oxidation of the surface of the epitaxial silicon layer 1102 is bonded to the glass substrate 1210. In this preferred embodiment, the other processes can be performed as in the embodiment shown in Figs.13A to 13E.

[0421] Hereinbelow, the present invention will be described in detail using concrete examples. However, the present invention is not limited thereto.

[Example 13]

[0422] A first p- or e-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter was anodized in an HF solution.

[0423] The anodization condition was as follows:

Current Density:	5 ($mA•cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0424] Subsequently, He^+ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the substrate at an acceleration voltage of 30keV. Then, the substrate was subjected to heat treatment at 850°C in the vacuum for 8 hours.

[0425] When the light of a mercury lamp was applied to the substrate, luminescence of the red light with a wavelength around 750nm was confirmed.

[Example 14]

[0426] Two first p-type (100) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared, and one of them was anodized in an HF solution.

[0427] The anodization condition was as follows:

Current Density:	5 ($mA•cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)

Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0428] He^+ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 30keV. Subsequently, phosphorus ions of $5x10^{14}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at an acceleration voltage of 100keV. Then, these substrates were subjected to the heat treatment at 850°C in the vacuum for 8 hours. Further, ITO electrodes were deposited on the surfaces.

[0429] When the voltage was applied between the Si substrates and the ITO electrodes, luminescence of a wavelength around 750nm was confirmed at the porous substrate, while luminescence was not confirmed at the other substrate.

[Example 15]

[0430] Two first p- or e-type (100) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared, and one of them was anodized in an HF solution.

[0431] The anodization condition was as follows:

Current Density:	5 ($mA•cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	20 (μm)
Porosity:	15 (%)

[0432] The anodized substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated

with a thermal-oxidized film. Subsequently, hydrogen ions of $5x10^{17}/cm^2$ were implanted all over the porous side of the porous substrate and all over the other substrate at an acceleration voltage of 0.76MeV.

[0433] When these substrates were subjected to the heat treatment at 1,000°C in the vacuum for 1 hour, the porous layer was separated uniformly all over the substrate with a thickness of about 1μm corresponding to the ion-implanted region, while a lot of swells like blisters were only formed at the non-porous substrate.

[Example 16]

[0434] The first p-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter was anodized in an HF solution.

[0435] The anodization condition was as follows:

Current Density:	5 ($mA•cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH$=1:1:1
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0436] The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation the pore inner walls of porous Si were coated with a thermally oxidized film. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxially grown by 0.1mm on porous Si. The growing conditions were as follows:

Source Gas:	SiH_2C1_2/H_2
Gas Flow Rate:	0.5/180 l/min
Gas Pressure:	80 Torr

Temperature:	900 °C
Growing Speed:	0.3 μm/min

[0437] He^+ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 30keV. Subsequently, phosphorus ions of $5x10^{14}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 100keV. Then, these substrates were subjected to heat treatment at 850°C in the argon atmosphere for 8 hours. Further, ITO electrodes were deposited on the surfaces.

[0438] When the voltage was applied between the Si substrate and the ITO electrode, luminescence of wavelength around 750nm was confirmed at the porous substrate.

[Example 17]

[0439] Two first p- or e-type (100) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0440] The anodization conditions were as follows:

Current Density:	5 ($mA•cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	3 (μm)
Porosity:	15 (%)

[0441] The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with

thermally oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxially grown by 0.15μm on porous Si. The growing conditions were as follows:

Source Gas:	SiH_2C1_2/H_2
Gas Flow Rate:	0.5/180 1/min
Gas Pressure:	80 Torr
Temperature:	950 °C
Growing Speed:	0.3 μm/min

[0442] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0443] Subsequently, He^+ ions of $5x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at an acceleration voltage of 50keV.

[0444] The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to heat treatment at 1,000°C for 2 hours to increase the bonding strength. Then, the two substrates were completely separated at a position corresponding to the projection range of the ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, no change on the outward appearance was caused on the substrate which was not subjected to the helium ion implantation, and the substrates remained bonded to each other. Thus, the porous Si substrate side of the bonded substrates (not subjected to the helium ion implantation) was ground using a grinder for the normal semiconductor to expose the porous Si layer. However, due to insufficient grinding accuracy, the whole porous layer could not be exposed.

[0445] Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:5) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed.

[0446] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the ratio of selective etching relative to the etching speed of the porous layer reaches no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0447] Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. No change was caused on the single-crystal Si layer even by the selective etching of porous Si.

[0448] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0449] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 18]

[0450] Two first p- or n-type (100) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in a HF solution.

[0451] The anodization conditions were as follows:

Current Density:	5 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0452] The substrates were oxidized at 400°C in an oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermally oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxially grown by 0.15μm on porous Si. The growing conditions were as follows. The accuracy of the film thickness was +2%.

Source Gas:	SiH_2C1_2/H_2
Gas Flow Rate:	0.5/180 1/min
Gas Pressure:	80 Torr
Temperature:	950 °C
Growing Speed:	0.3 μm/min

[0453] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0454] Subsequently, hydrogen ions of $5x10^{16}/cm^2$ were implanted into the porous side of only one of the substrates at an acceleration voltage of 50keV.

[0455] The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to heat treatment at 1,000°C for 2 hours to increase the bonding strength. Then, the two substrates were completely separated at a position corresponding to the projection range of the ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand,

no change in the outward appearance was caused on the substrate which was not subjected to the hydrogen ion implantation, and the substrates remained bonded to each other. The porous substrate side of the bonded substrates (not subjected to the hydrogen ion implantation) was ground using a grinder for the normal semiconductor to expose the porous layer. However, due to insufficient grinding accuracy, the thickness of the remaining porous layer was 1 to 9μm.

[0456] Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si regained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed.

[0457] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the ratio of selective etching relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0458] Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 10lnm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to influence of dispersion of thicknesses of porous silicon.

[0459] Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0460] When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0461] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and excellent crystallinity was maintained.

[0462] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0463] At the same time, the porous Si layer remaining on the Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and aqueous 30% hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as an etching stopper and fully removed, and the Si substrate could be again put into the porous-forming process.

[Example 19]

[0464] Two first p- or n-type (10) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

[0465] The anodization conditions were as follows:

Current Density:	5 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0466] The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermally oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was grown by 0.55μm on porous Si. The growing conditions were as follows. The accuracy of the film thickness was ±2%.

Source Gas:	SiH_2C1_2/H_2
Gas Flow Rate:	0.5/180 1/min
Gas Pressure:	80 Torr
Temperature:	900 °C
Growing Speed:	0.3 μm/min

[0467] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0468] Subsequently, hydrogen ions of $5x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at an acceleration voltage of 100keV.

[0469] The surface of the SiO_2 layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours to increase the bonding strength. The sufficient pressure is applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane. Then, the porous Si layer was divided into two at the ion-implanted region.

[0470] On the other hand, when the pressure was further applied to the substrate (not subjected to the hydrogen ion implantation), the porous layer was ruptured into two. However, when observing the divided porous layers, cracks were introduced into portions of the single-crystal Si layer so that the substrate could not be put into the subsequent process.

[0471] Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as an etching stopper and fully removed.

[0472] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0473] Specifically, the single-crystal Si layer having 0.5μm in thickness was formed on the Si oxidized film.

[0474] Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501nm ± 11 nm with the hydrogen ion implantation.

[0475] Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0476] When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0477] As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity property was maintained.

[0478] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0479] Using the CVD (chemical vapor deposition) method, single-crystal Si was again epitaxially grown by 0.55μm on porous Si remaining at the first substrate side. The growing conditions were as follows. The accuracy of the film thickness was ± 2%.

Source Gas:	SiH_2C1_2/H_2
Gas Flow Rate:	0.5/180 1/min
Gas Pressure:	80 Torr
Temperature:	900 °C
Growing Speed:	0.3 μm/min

[0480] When evaluating the crystal defect density of this single-crystal Si layer through the defect revealing etching, the defect density was about $1x10^3/cm^2$ and this substrate could be again put into the processes of ion implantation and bonding.

[0481] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 20]

[0482] Two first p- or n-type (100) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0483] The anodization conditions were as follows:

Current Density:	5 ($mA•cm^{-2}$)

Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0484] The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15μm on porous Si. The growing conditions were as follows. The accuracy of the film thickness was ± 2%.

Source Gas:	SiH_2C1_2/H_2
Gas Flow Rate:	0.5/180 l/min
Gas Pressure:	80 Torr
Temperature:	950 °C
Growing Speed:	0.3 μm/min

[0485] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0486] Subsequently, helium ions of $5x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

[0487] The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 400°C for 2 hours. The sufficient tensile force is applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane. Then, the two substrates were completely separated at a position corresponding to the projection range of the helium ion implantation. The separated surfaces were observed in detail using an

optical microscope, but exposed portions of the initial bonded interface were not found.

[0488] On the other hand, when the pressure was further applied to the substrate (not subjected to the helium ion implantation), the porous layer was ruptured into two. However, when observing the divided porous layers, cracks were introduced into portions of the single-crystal Si layer so that the substrate could not be put into the subsequent process.

[0489] Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as etching stopper and fully removed.

[0490] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0491] Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 101nm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution deteriorated due to influence of dispersion of thicknesses of porous silicon.

[0492] Thereafter, the heat treatment was performed at 1,100°C in a hydrogen atmosphere for 1 hour.

[0493] When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0494] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and excellent crystallinity was maintained.

[0495] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0496] At the same time, the porous Si layer remaining on the Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and aqueous 30% hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed, and the Si substrate could be again put into the porous-forming process.

[Example 21]

[0497] Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0498] The anodization conditions were as follows:

Current Density:	5 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0499] The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MBE (molecular beam epitaxy) method, single-crystal Si was epitaxial-grown by 0.5μm on porous Si. The growing conditions were as follows. The accuracy of the film thickness was ±2%.

Temperature:	700°C
Pressure:	1×10^{-9} Torr
Growing Speed:	0.1 nm/sec
Temperature:	950°C
Growing Speed:	0.3 μm/min

[0500] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0501] Subsequently, helium ions of $1 \times 10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at an acceleration voltage of 100keV.

[0502] The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to heat treatment at 300°C for 2 hours. The bonded two wafers were fixed by a vacuum chuck and applied with torsion and shearing forces in the horizontal direction relative to the main surface of the wafers. Then, the two substrates were completely separated at a position corresponding to the projection range of the helium ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found.

[0503] On the other hand, when the pressure was further applied to the substrate (not subjected to the helium ion implantation), the vacuum chuck was detached and the substrate could not be put into the subsequent process.

[0504] Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed.

[0505] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0506] Specifically, the single-crystal Si layer 0.1μm thick was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 10lnm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution deteriorated due to influence of dispersion of thicknesses of porous silicon.

[0507] Thereafter, heat treatment was performed at 1,100°C in a hydrogen atmosphere for 1 hour.

[0508] When evaluating the surface roughness using an interatomic force microscope, the mean square roughness of 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0509] As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and excellent crystalline properties were maintained.

[0510] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0511] At the same time, the porous Si layer remaining on the Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and aqueous 30% hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed, and the Si substrate could be again put into the porous-forming process.

[Example 22]

[0512] Two first p- or n-type (100) single-crystal Si substrates each being 625μm thick, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

[0513] The anodization conditions were as follows:

Current Density:	5 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0514] The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermally oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxially grown by 0.55μm on porous Si. The growing conditions was as follows. The accuracy of the film thickness was ± 2%.

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate:	0.5/180 1/min
Gas Pressure:	80 Torr
Temperature:	900°C
Growing Speed:	0.3 μm/min

[0515] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0516] Subsequently, hydrogen ions of $1x10^{18}/cm^2$ were implanted into the porous side of only one of the substrates at an acceleration voltage of 100keV.

[0517] The surface of the SiO_2 layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours to increase the bonding strength. Then, the porous Si layer was divided into two at the ion-implanted region.

[0518] On the other hand, no change was observed at the substrate which was not subjected to the helium ion implantation.

[0519] Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and aqueous 30% hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed.

[0520] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches no less than 10^5 and the etching amount (about several

tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0521] Specifically, the single-crystal Si layer 0.5μm thick was formed on the quartz substrate. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501nm ± 11nm with the hydrogen ion implantation. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0522] When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0523] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and excellent crystallinity was maintained.

[0524] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 23]

[0525] A first p- or n-type (100) single-crystal Si substrate being 625μm thick, 0.01Ω•cm in resistivity and 5 inches in diameter was prepared and anodized in an HF solution.

[0526] The anodization conditions were as follows:

Current Density:	5 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)

Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0527] The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, pore inner walls of porous Si were coated with thermally oxidized films. Using the MOCVD (metal organic chemical vapor deposition) method, single-crystal GaAs was epitaxially grown by lμm on porous Si. The growing conditions were as follows.

Source Gas:	$TMG/AsH_3/H_2$
Gas Pressure:	80 Torr
Temperature:	700°C

[0528] Subsequently, helium ions of $1x10^{18}/cm^2$ were implanted into the porous side of the substrate at an acceleration voltage of 100keV.

[0529] The surface of the GaAs layer and the surface of a separately prepared support Si substrate were overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to enhance the bonding strength. Then, the porous Si layer was divided into two at the ion-implanted region.

[0530] Thereafter, after removing the oxidized film on the inner walls of the porous Si layer using hydrofluoric acid, the porous Si was etched with a solution of ethylenediamine, pyrocatechol and water (ratio: 17ml:3g:8ml) at 110°C. Single-crystal GaAs remained without being etched so that porous Si was selectively etched using single-crystal GaAs as an etching stopper and fully removed.

[0531] The etching speed of single-crystal GaAs relative to the etching liquid is extremely low so that the thickness reduction can be ignored from a practical point of view.

[0532] Specifically, the single-crystal GaAs layer having 1μm in thickness was formed on the Si substrate. No change was caused on the single-crystal GaAs layer even by the selective etching of porous Si.

[0533] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the GaAs layer and excellent crystallinity was maintained.

[0534] By using the Si substrate with the oxidized film as the support substrate, GaAs on the insulating film could also be produced similarly.

[Example 24]

[0535] A first p- or n-type, (100) single-crystal Si substrate being 625μm thick, 0.01Ω•cm in resistivity and 5 inches in diameter was prepared and anodized in an HF solution.

[0536] The anodization conditions were as follows:

Current Density:	10 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	24 (minutes)
Thickness of Porous Si:	20 (μm)
Porosity:	17 (%)

[0537] The substrate was oxidized at 400°C in the oxygen atmosphere for 2 hours. Through the oxidation, the pore inner walls of porous Si were coated with thermally oxidized films. Using the MBE (molecular beam epitaxy) method, single-crystal AlGaAs was epitaxially grown by 0.5μm on porous Si.

[0538] Subsequently, helium ions of $1x10^{18}/cm^2$ were implanted into the porous side of the substrate at an acceleration voltage of 100keV.

[0539] The surface of the AlGaAs layer and the surface of a separately prepared support substrate of low melting point glass were overlapped and abutted with each other, and subjected to the heat treatment at 500°C for 2 hours. Through this heat treatment, the substrates were firmly bonded with each other.

[0540] When sufficient pressure was applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane, the porous Si layer was divided into two at the ion-implanted region.

[0541] Thereafter, porous Si was etched with a hydrofluoric acid solution. Single-crystal AlGaAs remained without being etched so that porous Si was selectively etched using single-crystal AlGaAs as an etching stopper and fully removed.

[0542] The etching speed of single-crystal AlGaAs relative to the etching liquid is extremely low so that the thickness reduction can be ignored from a practical point of view.

[0543] Specifically, the single-crystal AlGaAs layer 0.5μm thick was formed on the glass substrate. No change was caused on the single-crystal AlGaAs layer even by the selective etching of porous Si.

[0544] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the AlGaAs layer and excellent crystallinity was maintained.

[Example 25]

[0545] A first p- or n-type (100) single-crystal Si substrate with both sides polished and being 625μm 0.01Ω•cm in resistivity and 6 inches in diameter was prepared and anodized at both sides thereof in an HF solution. The anodization conditions were as follows:

Current Density:	5 ($mA•cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH$=1:1:1
Time:	12 x 2 (minutes)
Thickness of Porous Si:	10 (μm) for each side
Porosity:	15 (%)

[0546] The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermally oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxially grown by lμm on porous Si formed at each side. The growing conditions were as follows.

Source Gas:	SiH_2Cl_2/H_2
Gas Flow Rate:	0.5/180 1/min
Gas Pressure:	80 Torr
Temperature:	950°C
Growing Speed:	0.3 μm/min

[0547] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0548] Subsequently, hydrogen ions of $1x10^{18}/cm^2$ were implanted into the porous layers at an acceleration voltage of 100keV.

[0549] The surfaces of the SiO_2 layers and the surfaces of separately prepared two support Si substrates each formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to heat treatment at 600°C for 2 hours

to achieve bonding. Then, the porous Si layer was divided into two at the ion-implanted region.

[0550] Thereafter, the porous Si layer was agitated in a mixed solution (1:5) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed.

[0551] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0552] Specifically the two single-crystal Si layers each 1 μm thick were simultaneously formed on the Si oxidized films. No change was caused on the single-crystal Si layers even by the selective etching of porous Si.

[0553] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and excellent crystallinity was maintained.

[0554] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 26]

[0555] Two first p- or n-type (100) single-crystal Si substrates each 625μm thick, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

[0556] The anodization conditions were as follows:

Current Density:	5 ($mA \cdot cm^{-2}$)
Anodization Solution:	$HF:H_2O:C_2H_5OH=1:1:1$
Time:	12 (minutes)
Thickness of Porous Si:	10 (μm)
Porosity:	15 (%)

[0557] The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was grown by 0.55μm on porous Si. The growing conditions were as follows. The accuracy of the film thickness was ±2%.

Source Gas:	SiH_2Cl_2/H_2
Gas Flow Rate:	0.5/180 1/min
Pressure:	80 Torr
Temperature:	900°C
Growing Speed:	0.3 μm/min

[0558] Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0559] Subsequently, hydrogen ions of $1x10^{18}/cm^2$ were implanted into the porous side of only one of the substrates at an acceleration voltage of 100keV.

[0560] The surface of the SiO_2 layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the bonding strength. Subsequently, the wave

energy such as the ultrasonic wave was applied to the substrates. Then, the porous Si layer was divided into two at the ion-implanted region.

[0561] On the other hand, no change was observed at the substrate which was not subjected to the hydrogen ion implantation.

[0562] Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selectively etched using single-crystal Si as an etching stopper and fully removed.

[0563] The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0564] Specifically, the single-crystal Si layer 0.5μm thick was formed on the quartz substrate. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501nm ± 11nm with the hydrogen ion implantation. Thereafter the heat treatment was performed at 1,100°C in a hydrogen atmosphere for 1 hour.

[0565] When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0566] As a result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0567] Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0568] The single-crystal Si substrate was reused as a single-crystal Si substrate after removing remaining porous Si and performing surface-polishing to provide a mirror finished surface.

[0569] Recently, Sakaguchi et al. reported a method for reusing the first substrate, which was consumed in the above bonding method (Japanese Patent Application No. 07-045441 (1995)).

[0570] They employed the following method in place of the step of thinning the first substrate from the back surface by the method of grinding, etching, and the like to expose porous Si in the bonding plus etchback process using porous Si as described above.

[0571] A surface layer of first Si substrate 251 is made porous to obtain a porous layer 252, a single-crystal Si layer 253 is formed thereon, and this single-crystal Si layer 253 and first Si substrate is bonded through an insulating layer 255 with a principal surface of another second Si substrate 254 (Fig. 17). After this, the bonding wafer is divided at the porous layer (Fig. 18) and the porous Si layer exposed in the surface on the second Si substrate side is selectively removed, thereby forming an SOI substrate (Fig. 19).

[0572] Division of the bonding wafer is effected by using a method for breaking the porous Si layer, for example, either one of a method for applying sufficient

tension or pressure perpendicularly to and uniformly in the surface of the bonding wafer, a method for applying wave energy of ultrasonic wave or the like, a method for exposing the porous layer on the side face of wafer, etching some of the porous layer, and inserting an edge of a razor into the porous layer, a method for exposing the porous layer on the side face of wafer, infiltrating a liquid such as water into the porous Si layer, and thereafter expanding the liquid by heating or cooling the entire bonding wafer, and a method for applying force horizontally onto the second (or first) substrate relative to the first (or second) substrate, or the like.

[0573] These methods are all based on an idea that the mechanical strength of porous Si is sufficiently weaker than bulk Si, though depending upon its porosity. For example, with a porosity of 50%, the mechanical strength of porous Si may be considered to be half that of bulk Si. Namely, when compression, tension or shear force is exerted on the bonding wafer, the porous Si layer is broken first. With a greater porosity, the porous layer can be broken by a weaker force.

[0574] However, when force is exerted vertically or horizontally on the surface of wafer, the wafer is sometimes elastically deformed, thereby failing to properly exert force on the porous layer. This is because the observed semiconductor substrate is not a perfectly rigid body, but rather is an elastic body, and this also depends on the method of supporting a given wafer.

[0575] Similarly, with the method for inserting an edge of a razor or the like through the side surface of wafer, the yields were extremely lowered in some cases where the thickness of the razor was not sufficiently thin or where the razor did not have sufficiently high rigidity. Also, the razor was not able to be inserted uniformly from the periphery or the force was exerted from the outside on the bonding wafer. As a result, if the bond strength of the bonding surface was weaker than the strength of the porous Si layer or if there existed a locally weak portion,

the two wafers were split at the bonding surface, thereby sometimes failing to achieve the initial purpose.

[0576] Accordingly, a desire exists for a method for fabricating SOI substrates of sufficient quality with good reproducibility and, at the same time, realizing conservation of resources and reduction of cost by re-use of a wafer or the like.

[0577] The bulletin of Japanese Laid-open Patent Application No. 5-211128 (1993) describes a proposal for a method for forming a bubble layer by ion implantation, annealing it to cause rearrangement of crystal and cohesion of bubbles, and dividing the wafer through the bubble layer, wherein optimization of annealing is not easy and is carried out at low temperatures of 400 to 600°C. Annealing at such low temperatures cannot suppress generation of voids as described above, and the voids once generated cannot be nullified even with re-annealing at high temperature after thinning. Namely, the decrease in the number and size of voids is a phenomenon that occurs when the two wafers are annealed at high temperature in the bonded state, and high-temperature annealing after thinning will increase the strength of the adhesive portion, but will not decrease the voids.

[0578] The above description concerns the problems related to the SOI technology by bonding. There are also demands as to the SOI technology regarding formation of a single-crystal layer on a light transparent substrate, formation of a compound semiconductor layer on a substrate, and so on, for the following reasons:

[0579] The light transparent substrate is important in constructing contact sensors which serve as light receiving elements, and projection type liquid crystal image display devices. Further, high-performance drive elements are necessary for realizing higher-density, higher-resolution, and higher-definition of pixels (picture elements) in the sensors and display devices. As a result, the devices provided on

the light transparent substrate need to be fabricated using a single-crystal layer having excellent crystallinity. Use of the single-crystal layer enables peripheral circuits for driving the pixels and circuits for image processing to be incorporated in the same substrate as the pixels, thereby realizing size reduction and speed enhancement of a given chip.

[0580] However, the light transparent substrate typified by glass has disorderliness as to its crystal structure in general, and a thin Si layer deposited thereon is an amorphous layer or, at best, a polycrystal layer, reflecting the disorderliness of the substrate. High-performance devices cannot be fabricated of such a substrate. Namely, because of a crystal structure with many imperfections, it is not easy to fabricate drive elements of amorphous and polycrystal Si having sufficient performance that is required now or in the future. It is because the crystal structure of the substrate is amorphous, and simple deposition of Si layer will not yield a single-crystal layer with good quality.

[0581] On the other hand, substrates of compound semiconductor are necessary and indispensable for fabricating devices of compound semiconductor, but the substrates of compound semiconductor are expensive and it is very difficult to form a large area of compound semiconductor. For these reasons, attempts have been made to heteroepitaxially grow a compound semiconductor of GaAs or the like on the Si wafer, which can be fabricated as a large-area wafer.

[0582] However, the thus grown film has poor crystallinity because of differences of lattice constant and coefficient of thermal expansion and it is thus very difficult to apply it to devices.

[0583] It is, therefore, an object of the present invention to provide a process for fabricating a film with good crystallinity and to provide a process for fabricating a semiconductor substrate, which can effectively use the semiconductor substrate as

a material and which can suitably achieve conservation of resources and reduction of cost.

[0584] In the present invention, the porous Si layer is oxidized from the periphery of wafer, utilizing enhanced oxidation of porous Si. Volume expansion of porous Si increases from the center toward the periphery, and the present invention thus has the same effect as porous Si as if uniformly wedged from the periphery. In that case, the internal pressure is exerted on only the porous Si layer and the wafer is divided in the porous Si layer throughout the entire surface. This provides a fabrication process for a semiconductor substrate which solves the various problems discussed previously.

[0585] The principle of division by oxidation as a basis of the present invention will be described with reference to Fig. 20 to Fig. 22. In Fig. 20 to Fig. 22, reference numeral 211 designates a first Si single-crystal substrate; 212, a porous Si layer; 213, a non-porous thin film; 214, an insulating layer; 215, a second substrate; and 216, an oxidized porous Si layer. Although Fig. 20 to Fig. 22 illustrate an embodiment in which the insulating layer has been formed on the surface of the second substrate, it may be formed on the first substrate or both the first and second substrates. There are some cases such as GaAs on a Si p-n junction, where the insulating layer has been formed on neither of the substrates. Fig. 20 shows a bonding substrate immediately before oxidation. The side surface of porous Si is exposed. The side surface of porous Si is also normally covered by a non-porous thin film, and it is necessary to make the side surface exposed after or before bonding. When this bonding substrate is oxidized, enhanced oxidation starts from the side surface of porous Si because of the enormous surface area of porous Si. The volume expands 2.27 times when Si turns to SiO_2. Thus, if the porosity is not more than 56%, then the volume of the oxidized, porous Si layer will expand. The nearer the position to the center of the wafer, the lower the degree of oxidation. Thus, the volume expansion of the oxidized porous Si layer

near the side surface of the wafer becomes greater as shown in Fig. 21. This is just the same condition as if wedges are driven into the porous Si layer from the side surface of the wafer, and the internal pressure is exerted on only the porous Si layer, so that force acts so as to divide the substrate in porous Si. In addition, since oxidation uniformly progresses at the periphery of the wafer, the bonding wafer will be split equally from the circumference of the wafer. As a result, the wafer is divided as shown in Fig. 22. This oxidation step is a step used in the normal Si-IC processes and thus requires neither special facilities nor special techniques such as careful insertion of an edged tool.

[0586] The bonding substrate has a multi-layered structure, and, thus, if it has an interface of low strength or a locally weak region, the method of splitting at porous Si by external pressure would cause splitting at the weak portion. The present invention permits the internal pressure to be exerted on only the porous Si layer, utilizing one step, oxidation, with excellent uniformity of the normal Si-IC processes and combining the enhanced oxidizability of porous Si, volume expansion of porous Si, and fragility of porous Si, whereby the wafer can be divided with good controllability in the porous Si layer.

[0587] After the residual porous Si and oxidized porous Si layer is removed from the first Si substrate thus separated by the above method of the present invention, the first Si substrate is subjected to a surface flattening process if surface flatness thereof is insufficient. Then the first Si substrate can be reused again as a first Si layer or as a next second substrate.

[0588] The surface flattening process may be the method of polishing, etching, or any other method used in the normal semiconductor processes, but may be annealing in an atmosphere containing hydrogen. By properly selecting the conditions for this annealing, the substrate can be flattened so as to expose atomic steps locally. The annealing in the atmosphere containing hydrogen may be

carried out, for example, under such conditions as H_2 100%, 1100°C, 2 hours; H_2/Ar = 20/80, 1150°C, 1 hour; or H_2 100%, 1050°C, 2 hours.

[0589] Since the present invention permits a large area to be divided en bloc through the porous layer, it can omit the grinding, polishing, and etching steps that were conventionally essential for removing the first substrate to expose the entire surface of porous Si layer, thus decreasing processing steps.

[0590] When the substrate separated is repetitively used as a first Si substrate, this first Si substrate can be reused any number of times before it becomes unusable in the aspect of mechanical strength.

[0591] Further, since the conventional fabrication of a bonding substrate employs the method for successively removing the first Si substrate from one side thereof by grinding and etching, it is impossible to bond both surfaces of the first Si substrate to respective support substrates, thereby effectively utilizing the two surfaces. In contrast, according to the present invention, the first Si substrate, except for the surface layer, is maintained in its original state, and thus, by using both surfaces of the first Si substrate as principal surfaces and bonding the two surfaces to the respective support substrates, two substrates can be fabricated simultaneously by bonding, dividing, and thinning from one first Si substrate, thereby decreasing steps and improving productivity. Of course, the first Si substrate separated can be reused.

[0592] In other words, the present invention provides the Si single-crystal layer or the compound semiconductor single-crystal layer with the remarkably reduced number of imperfections on the insulator by using a Si single-crystal substrate in an economically desirable manner, which results in uniform flatness across a large area and excellent crystallinity, by removing the portion from its one surface to the

active layer and leaving the Si or compound semiconductor active layer formed in the surface.

[0593] The present invention provides a fabrication process for a semiconductor substrate superior with respect to productivity, uniformity, controllability, and cost in obtaining the Si or compound semiconductor single-crystal layer with excellent crystallinity equivalent to that of a single-crystal wafer, on a transparent substrate (light transparent substrate).

[0594] Also, the present invention provides a fabrication process for a semiconductor substrate that can replace the expensive SOS or SIMOX for fabricating large-scale integrated circuits of the SOI structure.

[0595] The present invention can form a single-crystal compound semiconductor layer with good crystallinity on porous Si, can transfer the semiconductor layer onto an economically desirable and large-area insulating substrate, and can form the compound semiconductor layer with good crystallinity on the insulating substrate while restraining the differences in lattice constant and coefficient of thermal expansion, which were problems in the prior art.

[0596] Further, removal of the porous Si layer of the present invention can also be done by selective polishing, using the single-crystal layer as a polishing stopper because porous Si has low mechanical strength and enormous surface area.

[0597] The present invention may combine anodization with ion implantation to make the porosity of the side surface small and the porosity of the central part large, thereby making the volume expansion of the side surface greater and the strength of the central part low so as to facilitate peeling.

[0598] In the present invention, a layer of a material having a smaller coefficient of thermal expansion than that of Si is formed at least on one side of the outer surfaces of the bonding substrate before splitting by oxidation (or possibly before bonding), whereby at temperatures during oxidation, Si becomes more likely to expand and thus stress acts in the wafer peeling directions in the peripheral region of the bonding wafer, facilitating occurrence of the wedge effect by oxidation.

[0599] The present invention simultaneously solves the various problems discussed previously by the above-stated enhanced oxidation and volume expansion of porous layer effected uniformly from the periphery of wafer.

[0600] Uhlir et al. discovered porous Si during the research process on electrolytic polishing of semiconductor in 1956 (A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956)). Porous Si can be formed by anodizing an Si substrate in HF solution. Unagami et al. studied dissolution of Si in the anodization and reported that the anode reaction of Si in HF solution required holes and that the reaction was as follows (T. Unagami, J. Electrochem. Soc., vol. 127, 476 (1980)):

$$Si + 2HF + (2 - n)e^+ \rightarrow SiF_2 + 2H^+ + ne^-$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (4 - \lambda)e^+ \rightarrow SiF_4 + 4H^+ + \lambda e^-$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

[0601] Here, e^+ and e^- represent a hole and an electron, respectively. Further, each of n and λ is the number of holes necessary for one atom of Si to dissolve, and it is reported that porous Si is formed when the condition of $n > 2$ or $\lambda > 4$ is satisfied.

[0602] From the foregoing, p-type Si including holes can be changed to porous Si, but n-type Si cannot. The selectivity in this porous Si formation was verified by

Nagano et al. and Imai (Nagano, Nakajima, Anno, Onaka, and Kajiwara, technical research report, the Institute of Electronics, Information and Communication Engineers (IEICE), vol. 79, SSD 79-9549 (1979)) and (K. Imai, Solid-State Electronics, vol. 24, 159 (1981)).

[0603] There is, however, another report telling that heavily doped n-type Si can be changed to porous Si (R. P. Holmstrom and J. Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983)), and it is thus important to select a substrate that can realize porous Si formation without adhering to the difference between p-type and n-type.

[0604] Porous Si can be formed by anodization of the Si substrate in HF solution. The porous layer has a spongelike structure in which pores with diameters ranging approximately from 10^{-1} to 10 nm are arranged at intervals of about 10^{-1} to 10 nm. The density thereof can be changed in the range of 2.1 to 0.6 g/cm^3 by changing the concentration of HF solution in the range of 50 to 20% or by changing the current density, in comparison with the density of single-crystal Si 2.33 g/cm^3. Namely, the porosity can vary. Although the density of porous Si is below half that of single-crystal Si as described, it maintains the single crystal property and it is also possible to epitaxially grow a single-crystal Si layer on the porous layer. However, temperatures over 1000°C cause rearrangement of internal pores, which will impair the characteristic of enhanced etching. Therefore, the epitaxial growth of a Si layer is preferably low temperature growth selected from molecular beam epitaxial growth, plasma enhanced CVD, low pressure CVD, photo assisted CVD, bias sputter process, liquid phase growth, and so on. However, high-temperature growth is also possible, if a protective film is preliminarily formed over the pore walls of the porous layer by a method of low-temperature oxidation or the like.

[0605] Since a lot of pores are formed inside the porous layer, the density of the porous layer decreases by half or more. As a result, the surface area significantly increases as compared with the volume, and thus its chemical etching rate is

remarkably enhanced as compared with the etching rates of a normal single-crystal layer.

[0606] The mechanical strength of porous Si is lower than that of bulk Si, though it depends upon the porosity. For example, if the porosity is 50%, the mechanical strength can be considered to be half that of bulk. Namely, when compression, tension or shear force is exerted on the bonding wafer, the porous Si layer will be broken first. When porosity increases, the porous layer can be broken by weaker force.

[0607] It is reported that after ions of helium or hydrogen are implanted into bulk Si, followed by annealing, micro-cavities with diameters of several nm to several ten nm are formed in the density of even $10^{16\text{-}17}/cm^3$ in the implant region (for example, A. Van Veen, C. C. Griffioen, and J. H. Evans, Mat. Res. Soc. Symp. Proc. 107 (1988, Material Res. Soc. Pittsburgh, Pennsylvania) p. 449). Research was recently on utilization of the micro-cavities as gettering sites of metal impurities.

[0608] V. Raineri and S. U. Campisano implanted helium ions into bulk Si and annealed it to form the cavities. Thereafter, they formed a groove in the substrate to expose the side surface of the cavities and subjected it to oxidation. As a result, the cavities were selectively oxidized to form a buried, oxidized Si layer. Namely, they reported formation of the SOI structure thereby (V. Raineri, and S. U. Campisano, Appl. Phys. Lett. 66 (1995) p. 3654). Their method, however, failed to form the SOI structure over the entire surface of substrate because the thicknesses of the surface Si layer and buried, oxidized Si layer are limited to those that can effect both the formation of cavities and relaxation of stress introduced due to volume expansion upon oxidation together and because formation of a groove is necessary for selective oxidation. Such formation of cavities has been reported as a phenomenon occurring with injection of a light element into metal,

together with the swell and peeling phenomena of these cavities, as a part of research related to the first wall of a fusion reactor.

[0609] The second substrate may be selected, for example, from a Si substrate, a Si substrate with a oxidized Si film formed thereon, light transparent substrates such as a quartz substrate (silica glass) or a glass substrate, and metal substrates, but it is not limited particularly to these.

[0610] The thin film formed on the porous Si layer on the first substrate may be selected, for example, from metal thin films and carbon thin films as well as non-porous single-crystal Si and the compound semiconductors such as GaAs or InP, but it is not limited to these. Further, it is not essential that the thin film of these be formed over the entire surface, and it may be partially etched by a patterning process.

[0611] The bonding wafer of Si has advantages of being oxidized at high temperatures and simultaneously annealed at high temperatures for reduction of voids.

[0612] Embodiments of the present invention will be explained.

[Embodiment 14]

[0613] As shown in Fig. 23, a first Si single-crystal substrate 221 is first prepared and then at least one non-porous thin film 223 and a porous Si layer 222 immediately under it are formed over the outermost surface layer of the principal surface thereof. A procedure for fabricating the non-porous thin film 223 and porous Si layer 222 is either one selected from the following procedures:

a) forming the porous Si layer 222 by anodization and forming the non-porous thin film 223;

b) implanting ions of at least one element selected from rare gases, hydrogen, and nitrogen into the substrate to simultaneously form the porous Si layer 222 and the non-porous thin film 223; and

c) in addition to a), further implanting ions of at least one element selected from rare gases, hydrogen and nitrogen into the substrate to make another region with a different porosity.

[0614] The non-porous thin film 223 is arbitrarily selected from single-crystal Si, polycrystal Si, amorphous Si, or metal films, compound semiconductor thin films, superconductive thin films, and so on. Even the device structure of MOSFET or the like may be formed. Further, formation of SiO_2 as an outermost layer is preferred for the reason that the interface state of the bonding interface can be separated away from the active layer (though SiO_2 does not always have to be provided). Observation of the implant layer with a transmission electron microscope confirms that an infinite number of micro-cavities are formed. There are no specific limitations on the charge state of implant ions. The acceleration energy is so set that the projected range is coincident with the depth desired to implant. The size and density of micro-cavities formed vary depending upon an implant amount, but the density is approximately $1 \times 10^{14}/cm^2$ or more, more preferably $1 \times 10^{15}/cm^2$. If the projected range is desired to be set deeply, channeling ion implantation may be applied. After implantation, annealing is carried out as occasion demands. As shown in Fig. 24, the second substrate 224 is made in close contact with the surface of the first substrate at room temperature. After that, bonding may be enhanced by anodic bonding, pressing, or annealing if necessary, or a combination thereof.

[0615] If single-crystal Si is deposited, it is preferred to form oxidized Si by a method of thermal oxidation or the like over the surface of single-crystal Si and then to bond it to the second substrate. The second substrate may be selected from Si, a substrate obtained by forming an oxidized Si film on an Si substrate, light

transparent substrates of quartz or the like, sapphire, and the like, but it is not limited to these. The point is that a surface thereof to be bonded is sufficiently flat.

[0616] The two substrates may be bonded in the three-plate laminate structure with an insulating thin plate therebetween.

[0617] A layer of a material having a smaller coefficient of thermal expansion than Si may be formed on at least one side of the outer surfaces of the bonding substrate before splitting by oxidation (or possibly before bonding). At temperatures during oxidation, Si becomes easier to expand and stress acts in the wafer peeling directions around the periphery of the bonding wafer, thereby supplementing the wedge effect by oxidation.

[0618] The side surface of the porous Si layer is made to be exposed by etching the non-porous thin film 223 after bonding, etching it before bonding, or preventing the non-porous thin film 223 from being formed on the side surface. The bonding substrate is oxidized to subject porous Si of the side surface to enhanced oxidation. (In the drawing, numeral 225 designates oxidized porous Si.) Then, as shown in Fig. 25, volume expansion of side-surface porous Si causes stress to act so as to peel the porous Si layer and, finally, to divide the substrate in the porous Si layer 222 (Fig. 26). The second substrate side has the structure of porous Si 222 + oxidized porous Si 225 / non-porous thin film (single-crystal Si layer, for example) 223 / second substrate 224.

[0619] Further, the porous Si 222 and oxidized porous Si 225 is selectively removed. Oxidized porous Si 225 is etched with hydrofluoric acid solution. When the non-porous thin film is of single-crystal Si, only porous Si 222 is etched by electroless wet chemical etching with at least one etchant selected from ordinary Si etchants, hydrofluoric acid being an etchant for selective etching of porous Si, a mixture solution obtained by adding at least one of alcohol (ethyl alcohol,

isopropyl alcohol, etc.) and hydrogen peroxide solution to hydrofluoric acid, buffered hydrofluoric acid, and a mixture solution obtained by adding at least one of alcohol and hydrogen peroxide to buffered hydrofluoric acid, thereby leaving the film preliminarily formed on the porous layer of the first substrate, on the second substrate. As detailed above, only porous Si can be selectively etched even with the ordinary Si etchant, because of the enormous surface area of porous Si. Alternatively, porous Si 222 is removed by selective polishing, using the non-porous thin film layer 223 as a polishing stopper.

[0620] When a compound semiconductor layer is formed on the porous layer, only porous Si 222 is chemically etched with an etchant having a faster etch rate of Si than that of the compound semiconductor, thereby leaving, and thus forming, the thinned single-crystal compound semiconductor layer 223 on the second substrate 224. Alternatively, porous Si 222 is removed by selective polishing, using the single-crystal compound semiconductor layer 223 as a polishing stopper.

[0621] Fig. 27 shows a semiconductor substrate obtained by the present invention. A non-porous thin film, for example, a single-crystal Si thin film 223, is formed, as thinned flatly and uniformly, in a large area throughout the entire region of wafer on the second substrate 224. If an insulating substrate is used as the second substrate 224, the semiconductor substrate thus obtained can be suitably used also from the viewpoint of fabrication of dielectric-isolated electronic devices.

[0622] The first Si single-crystal substrate 221 can be reused again as a first Si single-crystal substrate 221 or as a second substrate 224 after the residual porous Si and oxidized porous Si layer is removed and, if the surface thereof is too rough, after the surface thereof is flattened.

[Embodiment 15]

[0623] As shown in Fig. 28 to Fig. 32, the above step described in Embodiment 14 is applied to both surfaces of the first substrate with two second substrates, thereby fabricating two semiconductor substrates simultaneously.

[0624] In Fig. 28 to Fig. 32, reference numeral 231 designates a first Si single-crystal substrate; 232, porous Si layers provided on both principal surfaces of the first Si single-crystal substrate 231; 233, non-porous thin films provided on the porous Si layers 232; 234 and 235, second substrates; and 236, oxidized porous Si layers.

[0625] The first Si single-crystal substrate 231 can be reused again as a first Si single-crystal substrate 231 or as a second substrate 234 (or 235) after residual porous Si is removed or, if the surface is too rough, after the surface is flattened.

[0626] The support substrates 234, 235 do not have to be identical.

[0627] The non-porous thin-films 233 on both surfaces do not have to be identical.

EXAMPLES

[0628] Examples of the present invention will be described.

(Example 27)

[0629] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA•cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	11 (min)

Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0630] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growing rate:	0.3μm/min

[0631] Further, an SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0632] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with an SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0633] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0634] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in a mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer were selectively etched to be removed completely.

[0635] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0636] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0637] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with an atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0638] Observation of cross section with a transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0639] The present example showed an example in which the oxide film was formed in the surface of the epitaxial Si layer and in which the oxide film was also formed in the surface of the second substrate (i.e., the oxide film was formed in both substrates), but the same results were attained in the cases wherein the oxide

film was provided in either one substrate and wherein the oxide film was not provided in either substrate. However, as discussed previously, formation of the oxide film over the outermost layer of the epitaxial Si layer is preferable from the point that the interface state of the bonding interface is able to be separated away from the active layer.

[0640] In fact, it was also the case in the subsequent embodiments that the same results were attained in any cases wherein the oxide film was formed in both substrates, wherein the oxide film was formed in either one of the substrates, and wherein the oxide film was not formed in either substrate. Then, it is also the case that formation of the oxide film over the outermost layer of non-porous thin film (epitaxial Si layer) is preferable from the point that the interface state of the bonding interface can be separated away from the active layer.

(Example 28)

[0641] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 10 Ω•cm, and a SiO_2 layer of 100 nm was formed over the surface thereof by thermal oxidation. Hydrogen ions were implanted in 1 x $10^{17}/cm^2$ into the principal surface with the acceleration voltage of 50 keV applied. This resulted in forming a porous structure in the depth of near 0.5 μm below the surface by hydrogen bubbles.

[0642] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0643] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated

surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0644] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer were selectively etched to be removed completely.

[0645] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0646] Namely, the single-crystal Si layer was formed in the thickness of 0.5 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was within ±3%.

[0647] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0648] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 29)

[0649] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA•cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0650] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growing rate:	0.3μm/min

[0651] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0652] Then hydrogen ions were implanted in 1 x $10^{16}/cm^2$ into the principal surface with the acceleration voltage of 180 keV applied.

[0653] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover,

separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0654] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly into two substrates at a position corresponding to the projected range of hydrogen ion implantation in the porous Si layer after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0655] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0656] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0657] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0658] Further, it was annealed at 1100 °C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean

square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0659] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 30)

[0660] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω •cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	3 (min)
Thickness of porous Si:	3 (μm)
Porosity:	15 (%)

[0661] Further,

Current density:	30 ($mA \cdot cm^{-2}$)
Anodization solution:	HF: H_2O: C_2H_50H = 1:1:1
Time:	3 (min)
Thickness of porous Si:	10 (μm)
Porosity:	45 (%)

[0662] Further,

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	HF: H_2O: C_2H_50H = 1:1:1
Time:	3 (min)
Thickness of porous Si:	3 (μm)

Porosity:	15 (%)

[0663] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0664] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0665] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0666] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The portion with the higher porosity was structurally fragile, so that division started from that fragile portion. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0667] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0668] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0669] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0670] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0671] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 31)

[0672] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm,

and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0673] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0674] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0675] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with an SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0676] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated

surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0677] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0678] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0679] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0680] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0681] Observation of cross section with the transmission electron microscope resulted in confirming that no new, crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0682] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 32)

[0683] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0684] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 l/min
Gas pressure:	80 Torr
Temperature:	950 °C
Growth rate:	0.3 μm/min

[0685] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0686] Hydrogen ions were implanted in 1 x $10^{16}/cm^2$ in a region of the principal surface except for the peripheral 10 mm of wafer with the acceleration voltage of 150 keV applied. This implantation of hydrogen ions can realize a low porosity for the peripheral portion and a high porosity for the central portion, whereby in the oxidation process, the volume expansion of the peripheral portion becomes greater. Therefore, the central portion becomes weaker in strength and is thus easy to peel.

[0687] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0688] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly into two substrates at a position corresponding to the projected range of hydrogen ion implantation in the porous Si layer after 0.7 hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0689] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0690] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0691] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0692] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0693] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 33)

[0694] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0695] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 l/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0696] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0697] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared, after they were exposed to an oxygen plasma. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si. The oxygen plasma process can enhance the bonding strength, and if they are further heated at 300°C for about one hour after being exposed to the oxygen plasma, superimposed on each other, and contacted with each other, the bonding strength becomes much higher.

[0698] The bonding wafer was pyro-oxidized at 1100°C, and it was divided perfectly in the porous Si layer into two substrates after 0.7 hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0699] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0700] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0701] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm $\pm$ 3 nm.

[0702] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0703] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0704] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide

solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 34)

[0705] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 10 Ω•cm, and an SiO_2 layer of 100 nm was formed over the surface thereof by thermal oxidation. Hydrogen ions were implanted in 1 x $10^{17}/cm^2$ into the principal surface with the acceleration voltage of 25 keV applied. This resulted in forming a porous structure in the depth of near 0.3 μm below the surface by hydrogen bubbles.

[0706] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared, after they were exposed to a nitrogen plasma. After contact of the surfaces, the SiO_2 layer of 100 nm and the Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si. The nitrogen plasma process can enhance the bonding strength, and if they are further heated at 300°C for about one hour after being exposed to the nitrogen plasma, superimposed on each other, and contacted with each other, the bonding strength becomes much higher.

[0707] The bonding wafer was dry-oxidized at 1100°C, and it was divided perfectly in the porous Si layer into two substrates after two hours. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0708] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0709] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0710] Namely, the single-crystal Si layer was formed in the thickness of 0.2 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was within ±3 %.

[0711] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0712] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0713] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the

single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 35)

[0714] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15(%)

[0715] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 l/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0716] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0717] Hydrogen ions were implanted in 5 x $10^{16}/cm^2$ into the principal surface with the acceleration voltage of 180 keV applied.

[0718] Then the SiO_2 layer of 100 nm and the epitaxial Si layer in the side surface were removed to expose the porous Si layer.

[0719] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared, after they were exposed to a nitrogen plasma. The nitrogen plasma process can enhance the bonding strength, and if they are further heated at 300°C for about one hour after being exposed to the nitrogen plasma, superimposed on each other, and contacted with each other, the bonding strength becomes much higher.

[0720] The bonding wafer was pyro-oxidized at 900°C, and it was divided perfectly into two substrates at a position corresponding to the projected range of hydrogen ion implantation in the porous Si layer after two hours. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0721] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0722] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or

more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0723] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0724] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0725] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0726] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 36)

[0727] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to both-face anodization in HF solution. The conditions for

the anodization were as follows. The both-face anodization was carried out face by face for 11 minutes each.

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 x 2 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15(%)

[0728] This substrate was oxidized at 400°C in an oxygen ambient for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on each porous Si layer by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0729] Further, a SiO_2 layer of 100 nm was formed over the surface of each epitaxial Si layer by thermal oxidation.

[0730] The surfaces of the SiO_2 layers were laid on and made to contact respective surfaces of two Si substrates (second substrates) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layers of 100 nm and the epitaxial Si layers were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0731] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layers into three substrates after one hour. The separated

surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0732] After that, the porous Si and oxidized porous Si layers left on the side of the two second substrates were subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layers were selectively etched to be removed completely.

[0733] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0734] Namely, two of the single-crystal Si layer were formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0735] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0736] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0737] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 37)

[0738] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0739] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0740] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0741] Hydrogen ions were implanted in 1 x $10^{16}/cm^2$ into the principal surface with the acceleration voltage of 180 keV applied.

[0742] The surface of the SiO_2 layer was laid on and made to contact a surface of a quartz substrate (second substrate) prepared separately, after each surface was proposed to a nitrogen plasma. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si. The nitrogen plasma process can enhance the bonding strength, and if they are further heated at 300°C for about one hour after exposed to the nitrogen plasma, superimposed on each other, and contacted with each other, the bonding strength becomes much higher.

[0743] The bonding wafer was low-temperature-oxidized at 700°C, and it was divided perfectly into two substrates at a position corresponding to the projected range of hydrogen ion implantation in the porous Si layer after ten hours. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0744] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0745] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was practically ignorable (about several ten angstroms).

[0746] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film on the quartz substrate. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0747] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0748] The same results were obtained without forming the oxide film on the surface of the epitaxial Si layer.

[0749] The same results were obtained with low-melting point glass.

[0750] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 38)

[0751] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15(%)

[0752] This substrate was oxidized at 400°C in an oxygen ambient for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 1.05 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0753] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0754] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0755] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0756] After that, the porous Si and oxidized porous Si layer left on the second substrate side was subjected to selective polishing with single-crystal Si as a polishing stopper. Single-crystal Si was left without being polished, and with the single-crystal Si as a material of polishing stop, the porous Si and oxidized porous Si layer was selectively polished to be removed perfectly.

[0757] Namely, the single-crystal Si layer was formed in the thickness of 1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was ±3%.

[0758] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0759] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 39)

[0760] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm,

and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0761] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal GaAs was epitaxially grown in the thickness of 1 μm on porous Si by the MOCVD (Metal Organic Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	$TMG/AsH_3/H_2$
Gas pressure:	80 Torr
Temperature:	700°C

[0762] The surface of the GaAs layer was laid on and made to contact a surface of a Si substrate (second substrate) prepared separately and thereafter the epitaxial layer on the side surface of the bonding wafer was removed by etching, thereby exposing the edge of porous Si.

[0763] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0764] After that, the porous Si and oxidized porous Si layer left on the second substrate side was subjected to etching with ethylenediamine + pyrocatechol +

water (at a ratio of 17 m1:3 g:8 ml) at 110°C, after removing oxidized Si with HF. Single-crystal GaAs was left without being etched, and with the single-crystal GaAs as a material of etch stop the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0765] The etch rate of non-porous GaAs single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was practically ignorable (about several ten angstroms).

[0766] Namely, the single-crystal GaAs layer was formed in the thickness of 1 μm on Si.

[0767] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the GaAs layer and that good crystallinity was maintained.

[0768] Using an Si substrate with an oxide film as a support substrate, GaAs on the insulating film was also able to be fabricated in the same manner.

[0769] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 40)

[0770] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0771] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal AlGaAs was epitaxially grown in the thickness of 0.5 μm on porous Si by the MBE (Molecular Beam Epitaxy) process.

[0772] The surface of the AlGaAs layer was laid on and made to contact a surface of a glass substrate (second substrate) prepared separately and thereafter the epitaxial layer on the side surface of the bonding wafer was removed by etching, thereby exposing the edge of porous Si.

[0773] The bonding wafer was low-temperature-oxidized at 700°C, and it was divided perfectly in the porous Si layer into two substrates after ten hours. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0774] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal AlGaAs remained without being etched, and with the single-crystal

AlGaAs as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0775] The etch rate of non-porous AlGaAs single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0776] Namely, the single-crystal AlGaAs layer having the thickness of 0.5 μm was formed on the glass substrate.

[0777] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the AlGaAs layer and that good crystallinity was maintained.

[0778] After removing the residual porous Si and oxidized porous Si layer, the surface of the first Si single-crystal substrate was polished into a mirror surface and thereafter the first substrate was again used as a first Si single-crystal substrate.

(Example 41)

[0779] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 (mA•cm^{-2})
Anodization solution:	HF:H_2O:C_2H_5OH = 1:1:1
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0780] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0781] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0782] The surface of the SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, prepared separately.

[0783] Si_3N_4 was deposited in the thickness of 0.5 μm at a low temperature on both outer surfaces of the bonding wafer and thereafter the Si_3N_4 layer of 0.5 μm and the SiO_2 layer of 100 nm and the epitaxial Si layer on the side surface of the bonding wafer were removed by etching, thereby exposing the edge of porous Si. When Si_3N_4 is formed in this manner, because Si is easier to expand than Si_3N_4, stress acts in the wafer peeling directions in the peripheral region of wafer, which facilitates occurrence of the wedge effect by oxidation.

[0784] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after 0.8 hour. The separated surfaces were observed, showing that the central portion was found to remain

almost in its original state while porous Si of the wafer side surface was changed to SiO_2. The Si_3N_4 layer on the back surface may or may not be removed.

[0785] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0786] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0787] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0788] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with an atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0789] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0790] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. Thus, the first substrate of single-crystal Si was able to be put again into the porous layer forming step.

(Example 42)

[0791] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 (mA•cm^{-2})
Anodization solution:	HF:H_2O:C_2H_5OH = 1:1:1
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0792] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 l/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0793] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0794] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0795] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0796] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0797] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0798] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed

were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0799] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0800] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0801] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. After being polished, the first substrate was able to be put into the process as a second substrate this time.

(Example 43)

[0802] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to both-face anodization in HF solution. The conditions for the anodization were as follows. The both-face anodization was carried out face by face for 11 minutes each.

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 x 2 (min)
Thickness of porous Si:	12 (μm)

Porosity:	15 (%)

[0803] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on each porous Si layer by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 l/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0804] Further, a SiO_2 layer of 100 nm was formed over the surface of each epitaxial Si layer by thermal oxidation.

[0805] The surfaces of the SiO_2 layers were laid on and made to contact respective surfaces of two Si substrates (second substrates) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layers of 100 nm and the epitaxial Si layers were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0806] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layers into three substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0807] After that, the porous Si and oxidized porous Si layers left on the side of the two second substrates were subjected to selective etching with agitation in the

mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layers were selectively etched to be removed completely.

[0808] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0809] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0810] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0811] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0812] At the same time, the porous Si and oxidized porous Si layer left on the first substrate side was also subjected thereafter to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si was left without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely. After being polished, the

first substrate was able to be put into the process as one of the second substrates this time.

(Example 44)

[0813] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 10 Ω•cm, and an SiO_2 layer of 100 nm was formed over the surface thereof by thermal oxidation. Helium ions were implanted in 1 x $10^{17}/cm^2$ into the principal surface with the acceleration voltage of 100 keV applied. This resulted in forming a porous structure in the depth of near 0.5 μm below the surface by helium bubbles.

[0814] The surface of this SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, separately prepared. After contact of the surfaces, the SiO_2 layer of 100 nm and the epitaxial Si layer were removed by etching on the side surface of the bonding wafer, which exposed the edge of porous Si.

[0815] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0816] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0817] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0818] Namely, the single-crystal Si layer was formed in the thickness of 0.5 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was within ±3%.

[0819] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0820] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 45)

[0821] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH = 1:1:1$
Time:	11 (min)
Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0822] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0823] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0824] The surface of the SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, prepared separately, and thereafter a pulse voltage of ±500 V and cycles of 100 msec was applied thereto to enhance the bonding strength more. Further, the SiO_2 layer of 100 nm and the epitaxial Si layer on the side surface of the bonding wafer were removed by etching, thereby exposing the edge of porous Si.

[0825] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0826] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a

material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0827] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0828] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0829] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0830] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

(Example 46)

[0831] Prepared was a p-type or n-type 6-inch-diameter first (100) single-crystal Si substrate having the thickness of 625 μm and the specific resistance of 0.01 Ω•cm, and it was subjected to anodization in HF solution. The conditions for the anodization were as follows:

Current density:	7 ($mA \cdot cm^{-2}$)
Anodization solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Time:	11 (min)

Thickness of porous Si:	12 (μm)
Porosity:	15 (%)

[0832] This substrate was oxidized at 400°C in an oxygen atmosphere for one hour. This oxidation caused a thermally oxidized film to cover the internal walls of pores of porous Si. Single-crystal Si was epitaxially grown in the thickness of 0.15 μm on porous Si by the CVD (Chemical Vapor Deposition) process. The growth conditions were as follows:

Source gas:	SiH_2C1_2/H_2
Gas flow rate:	0.5/180 1/min
Gas pressure:	80 Torr
Temperature:	950°C
Growth rate:	0.3 μm/min

[0833] Further, a SiO_2 layer of 100 nm was formed over the surface of this epitaxial Si layer by thermal oxidation.

[0834] The surface of the SiO_2 layer was laid on and made to contact a surface of a Si substrate (second substrate) with a SiO_2 layer of 500 nm formed thereover, prepared separately, and thereafter a pressure of 1000 kg/cm^2 was applied thereto at room temperature perpendicularly to the bonding substrate to enhance the bonding strength more. Further, the SiO_2 layer of 100 nm and the epitaxial Si layer on the side surface of the bonding wafer were removed by etching, thereby exposing the edge of porous Si.

[0835] The bonding wafer was pyro-oxidized at 1000°C, and it was divided perfectly in the porous Si layer into two substrates after one hour. The separated surfaces were observed, showing that the central portion was found to remain almost in its original state while porous Si of the wafer side surface was changed to SiO_2.

[0836] After that, the porous Si and oxidized porous Si layer remaining on the second substrate side was subjected to selective etching with agitation in the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide solution. Single-crystal Si remained without being etched, and with the single-crystal Si as a material of etch stop, the porous Si and oxidized porous Si layer was selectively etched to be removed completely.

[0837] The etch rate of non-porous Si single crystal by the etchant was extremely low and the selectivity of the etch rate of the porous layer thereto was even 10^5 or more. Therefore, a decrease in film thickness of the non-porous layer was so small that the etch amount thereof was negligible (about several ten angstroms).

[0838] Namely, the single-crystal Si layer was formed in the thickness of 0.1 μm on the Si oxide film. Film thicknesses of the single-crystal Si layer thus formed were measured at 100 points across the entire surface, and uniformity of film thickness was 101 nm ± 3 nm.

[0839] Further, it was annealed at 1100°C in hydrogen for one hour. Surface roughness was evaluated with the atomic force microscope and the root mean square roughness in a region 50 μm square was approximately 0.2 nm, which was equivalent to those of Si wafers commercially available.

[0840] Observation of cross section with the transmission electron microscope resulted in confirming that no new crystal defects were introduced into the Si layer and that good crystallinity was maintained.

[0841] In each of the examples described above, the epitaxial growth on porous Si can be carried out by various methods including the MBE process, the sputter process, the liquid phase growth process, etc. as well as the CVD process without

having to be limited to the CVD process. Additionally, the selective etching solution of porous Si is not limited to the mixture solution of 49% hydrofluoric acid and 30% hydrogen peroxide, but may be a mixture solution of hydrofluoric acid and alcohol (ethyl alcohol, isopropyl alcohol, etc.), a mixture solution of buffered hydrofluoric acid and hydrogen peroxide, or a mixture solution of buffered hydrofluoric acid and alcohol. Further, porous Si can also be selectively etched with a mixture solution of hydrofluoric acid, nitric acid, and acetic acid because of its enormous surface area. Mixture ratios of the mixture solutions may be set arbitrarily and properly.

[0842] The other steps can also be carried out under various conditions without having to be limited to the conditions described in the above examples.